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LeCroy CORPORATION

Service Manual

7242/7242A/7242B
500 MHz 1 GS/s
Oscilloscope

June 1994

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LECROY 7242 SERIES SERVICE MANUAL

GENERAL INFORMATION

1.0 INTRODUCTION

This service manual contains information to maintain the LeCroy 7242 Series Plug-in for the 7200 Series Modular Digital Oscilloscope. The manual is divided into eight sections as follows:

1. **General Information**
   Contains the 7242 description, specifications, and characteristics.

2. **Performance Verification**
   Contains the performance tests necessary to verify instrument specifications, including recommended test equipment and test record form.

3. **Adjustments / Calibration**
   Contains the necessary procedures to adjust the instrument after servicing.

4. **Basic Operation / Block Diagrams**
   Contains operation descriptions and block diagrams for the instrument.

5. **Disassembly**
   Contains the disassembly and assembly procedures.

6. **Troubleshooting**
   Contains troubleshooting flowcharts to assist in the repair of the instrument.

7. **Schematics / Reference Diagrams**
   Contains schematics and component location diagrams.

8. **Parts List**
   Contains Replaceable and Full parts lists.

LeCroy

Innovators in Instrumentation

7242B Plug-In for the 7200 Series Modular Oscilloscope System

Main Features

- Up to 1 Mpoint/channel acquisition memory (optional), 200k/channel standard
- 2 independent channels, up to 4 channels per 7200 series mainframe
- 2 Gigasamples per second single shot sampling rate
- 20 Gigasamples per second repetitive sampling rate
- System bandwidth DC to 500 MHz
- Smart Trigger™ including glitch, pattern, slope, time/event qualified, TV
- Roll mode

General

The LeCroy 7242B, 2 channel plug-in is a high bandwidth, long record length plug-in for the LeCroy 7200 Series Modular Oscilloscope System. With a second 7242B plug-in, the 7200 Series provides 4 channels of simultaneous 1 GS/s digitizing.

The two input channels have flexible signal conditioning allowing the user to select 50 Ω or 1 MΩ input impedance with input sensitivities of 5 mV/div to 2.5 V/div.

The 7242B records 200,000 sample points on each input channel (1,000,000/channel optional). These long memories maintain full sample rate and usable bandwidth over a wide range of timebase settings.

By segmenting the memory, up to 4000 waveforms/channel can be acquired at high trigger rates.

Smart Trigger™ lets the user trigger on complex waveforms like glitches or bit streams, so rare or subtle events can be observed.

Refer to the LeCroy 7200A Operator's manual for information on operating and the LeCroy 7200A Programmer's manual for information on programming.

1.1 Initial Inspection

It is recommended that the shipment be thoroughly inspected immediately upon delivery to the purchaser. All material in the container should be checked against the enclosed packing list. LeCroy cannot accept responsibility for shortages in comparison with the packing list unless notified promptly. If the shipment is damaged in any way, please contact the Customer Service Department or your local field office immediately.

1.2 Warranty

LeCroy warrants its digitial oscilloscope products to operate within specifications under normal use for a period of two years from date of shipment. Spares, replacement parts and repairs are warranted for 90 days. The instrument's firmware is thoroughly tested and thought to be functional, but is supplied "as is" with no warranty of any kind covering detailed performance. Products not manufactured by LeCroy are covered solely by the warranty of the original equipment manufacturer.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the customer service department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and that the defect has not been caused by misuse, neglect, accident or abnormal conditions or operation.

LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all warranties, expressed or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental or consequential damages, whether in contract or otherwise.

1.3 Product Assistance

Answers to questions concerning installation, calibration and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977-6499, USA, Tel:(914) 578-6060 or 6061 and 2 rue du Pré-de-la-Fontaine, 1217 Meyrin 1, Geneva, Switzerland, Tel: (41) 22 / 719.21.11, or your local field engineering office.

1.4 Addresses

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Dewetron Elektronische Messgerate
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A-8044 Graz
Austria

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01610 Vantaa Finland

Avantec AS
Tventenveien 6
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Norway

Westplex Test & Measurement Pty
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Singapore 1336

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Kanata Ontario K2K 2M5
Canada

Woojoo Hi-Tech Corp
Donghyun Building
102-4 Moonjung-Dong, Songpa-Ku
C.P.O. Box 5809
Seoul 138 200 Korea

1.5 Maintenance Agreements

LeCroy offers a selection of customer support services. Maintenance agreements provide extended warranty and allow the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, enhancements and on-site repair are available through specific Supplemental Support Agreements.

1.6 Documentation Discrepancies

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product. There may be small discrepancies in the values of components for the purpose of pulse shape, timing, offset, etc.; and occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. In a similar way the firmware may undergo revision when the instrument is serviced. Should this be the case, manual updates will be made available as necessary.

1.7 Service Procedure

Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. LeCroy will repair or replace any product under warranty at no charge. The purchaser is only responsible for one-way transportation charges.

For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before repairs can be initiated. The customer will be billed for parts and labor for the repair, as well as for shipping.

1.8 Return Procedure

To determine your nearest authorized service facility, contact the Customer Service Department or your local field office. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user, and in the case of products returned to the factory, a Return Authorization Number (RAN). The RAN may be obtained by contacting the customer service department in New York, Tel: (914)578-6060 or 6061; in Geneva, Tel: (41)22/719.21.11 or your nearest sales office.

Return shipment should be made prepaid. LeCroy will not accept C.O.D. or Collect Return Shipments. Air-freight is generally recommended. Whenever possible, the original shipping carton should be used. If a substitute carton is used, it should be rigid and be packed such that the product is surrounded with a minimum of four inches of excelsior or similar shock-absorbing material. In addressing the shipment, it is important that the Return Authorization Number be displayed on the outside of the container to ensure its prompt routing to the proper department within LeCroy.

1.9 Safety Precautions

The following servicing instructions are for use by qualified personnel only. Do not perform any servicing other than contained in service instructions. Refer to procedures prior to performing any service.

Exercise extreme safety when testing high energy power circuits. Always turn the power OFF, disconnect the power cord, discharge the cathode ray tube before disassembling the instrument.

The W A R N I N G symbol used in this manual indicates dangers that could result on personal injury.

The C A U T I O N symbol used in this manual indicates conditions or practices that could damage the instrument.

1.10 Antistatic Precautions

CAUTION

Any static charge that builds on your person or clothing may be sufficient to destroy CMOS components, integrated circuits. In order to avoid possible damage, the usual precautions against static electricity are required.

- Handle the boards in antistatic boxes or containers with foam specially designed to prevent static build-up.
- Ground yourself with a suitable wrist strap.
- Disassemble the instrument at a properly grounded work station equipped with an antistatic mat.
- When handling the boards, do not touch the pins.
- Stock the boards in antistatic bags.

2.0 General Information

These test procedures are provided for the purpose of verifying the proper operation and basic specifications of the LeCroy 7200 series of mainframes and plugins. Performing these tests with traceable calibration standards is sufficient criteria for NIST certification.

These tests will test a 7242 series or 7234 module in a 7200 series mainframe. The calibration data may be logged to either a printer, a floppy or entered on the sample data sheets found at the end of this document..

2.1 Equipment Requirement List

7200 with software revision 2.0.0 or later
7200A with software revision 3.0.0 or later
NIST Calibration ICL program disk: PN 7200-NIST-DISK

Sinewave generator:
Marconi 2019A
Tektronix SG504
(or equivalent)

Square Wave Generator:
LeCroy 9210/ 9211 or 9214
Tektronix PG503
(or equivalent, with < 1nsec risetime)

Precision DC power Supply:
Datel DVC8500
Tektronix PS5004
(or Equivalent)

Power Meter:
HP 437B Power Meter
HP 8482A Head

2.2 7242/A/B & 7234 NIST CALIBRATION PROCEDURE

2.2.1 Setup

Place the 7242/A/B or 7234 under test into a 7200 series mainframe.

Execute default settings on the mainframe.

Load and Run ICL program "NIST" located on "7200 NIST DATA" disk.

If more than one module is found in the mainframe, a menu will be displayed as in Fig 2.1. The user will then select which module is to be tested.

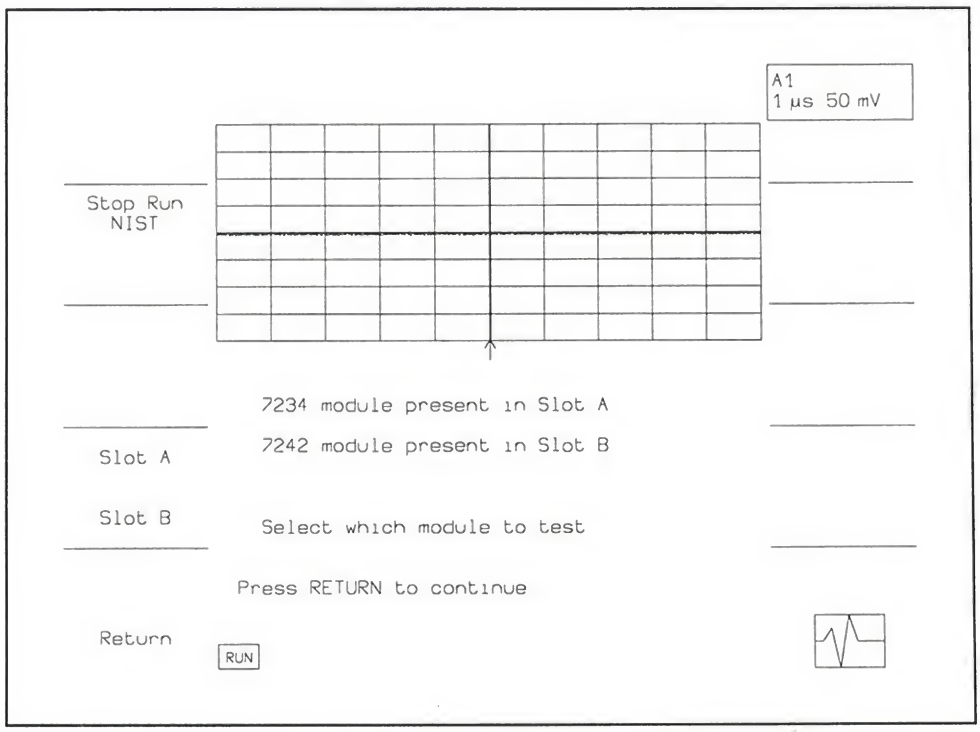


Fig 2.1

Next the LOGGING MENU will be displayed as in Fig 2.2.
Enter the serial number of the module by turning the inner cursor move knob. You will have the following choices of output type.

1) LOG TO PRINTER
2) LOG TO FLOPPY - Saves data to 3.5" floppy drive.The filename will be the serial number of the module under test (i.e. A96123.HCP).
3) NO LOG - Test results to screen only, the forms at the end of this document may be used as a data sheet.

Select the output type (default is NO LOG)

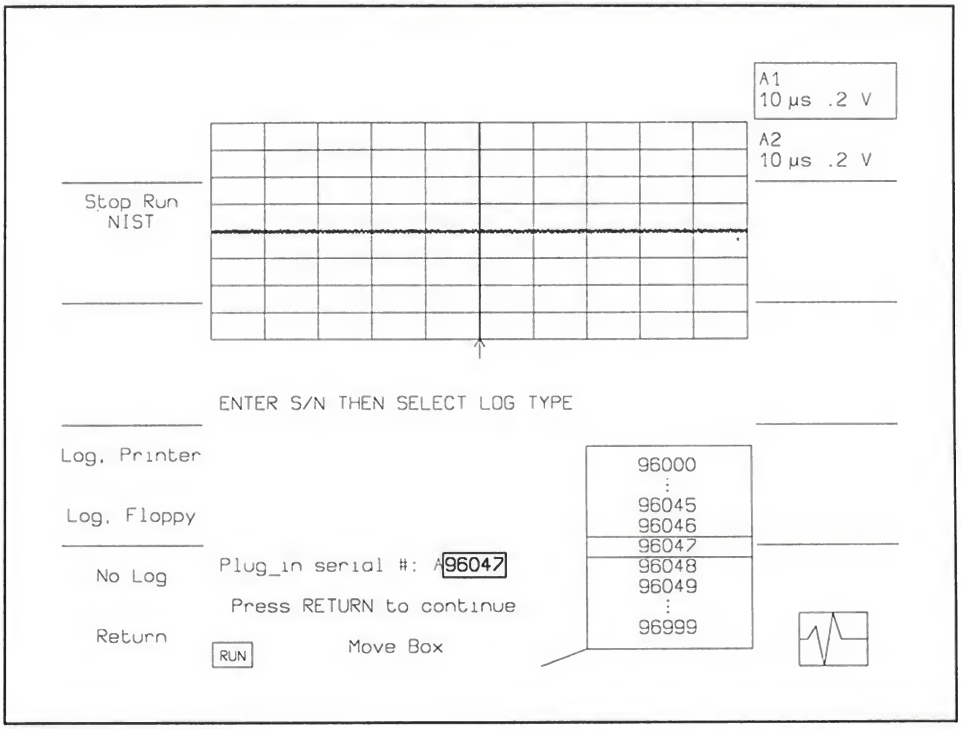


Fig 2.2

If the selected output type is Printer or Floppy, the hardcopy setup menu will appear on the screen (as in Fig 2.3) after the user pushes the softkey labeled "RETURN" to exit the logging menu. Here the user selects the setup configuration of the printer. Press RETURN to continue.

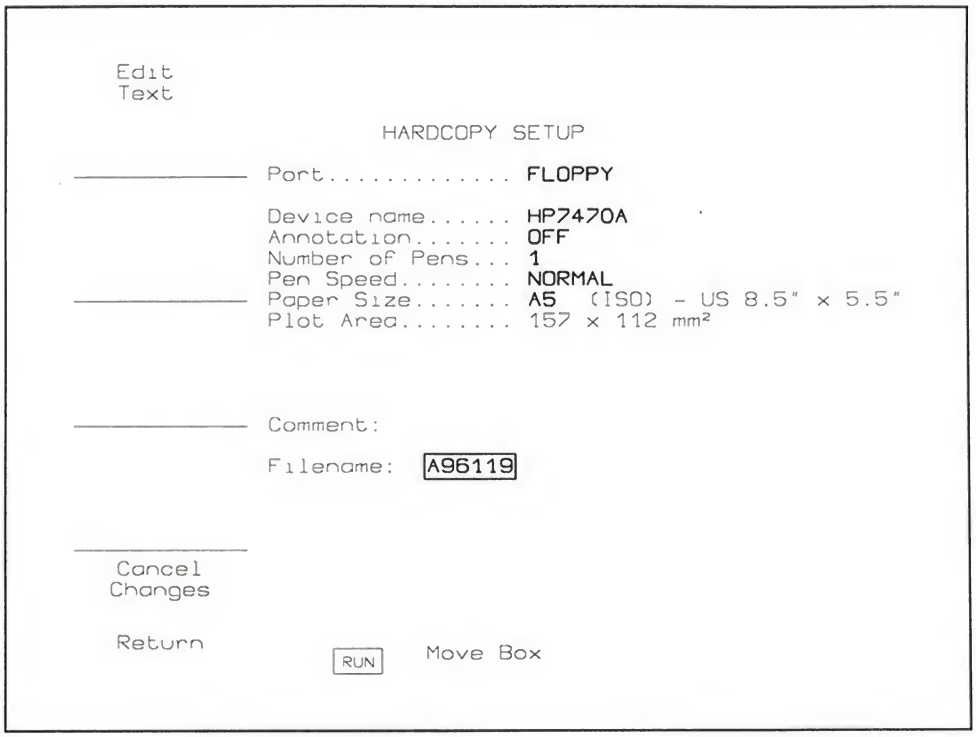


Fig 2.3

Next the user must select if the entire test is to be run by starting at the NOISE test or if tests are to be skipped by starting at one of the other listed tests. The order in which tests are run is NOISE, ADC, DCLIN, TRIGLEV, TIMEBASE, DELAY, IMPED and BW. Select from the choices and press the RETURN key to continue.

NOTE: *For each of the following tests, if a specification limit is exceeded, mark the failed range on the data sheet with an ASTERISK .*

2.2.2 BaseLine Noise

The NOISE test will check that the baseline noise does not exceed 1 mV(sdev) on the 5mV range on all channels.This test will be performed at all timebases between 200 us-20ns. The offset voltage will be set to zero volts.

- Connect 50Ω terminators to CH1, CH2, CH3, and CH4 inputs.
- If the selected LOG TYPE is either Printer or Floppy then the noise data will be collected automatically. If NO LOG was selected, when the test is complete the results will be displayed on the screen as in Fig 2.4. Record these results in table 2.1. Follow the displayed instructions.

The module controls will be set as follows:

Trace 1:	on :Ch1
Trace 2:	on :Ch2
Trace 3:	on :Ch3 (7234 only)
Trace 4:	on :Ch4 (7234 only)
Grid:	single
Input couplings CH1,CH2,CH3,CH4:	DC
Input gain:	5 mV/div
Time/div:	based on table

Trigger:

SMART trigger:	off
Source:	Line
Coupling:	AC
Level :	zero
MODE:	auto

Extended parameters are as follows:

T1 : SDEV
T2 : SDEV
T3 : SDEV (7234 only)
T4 : SDEV (7234 only)

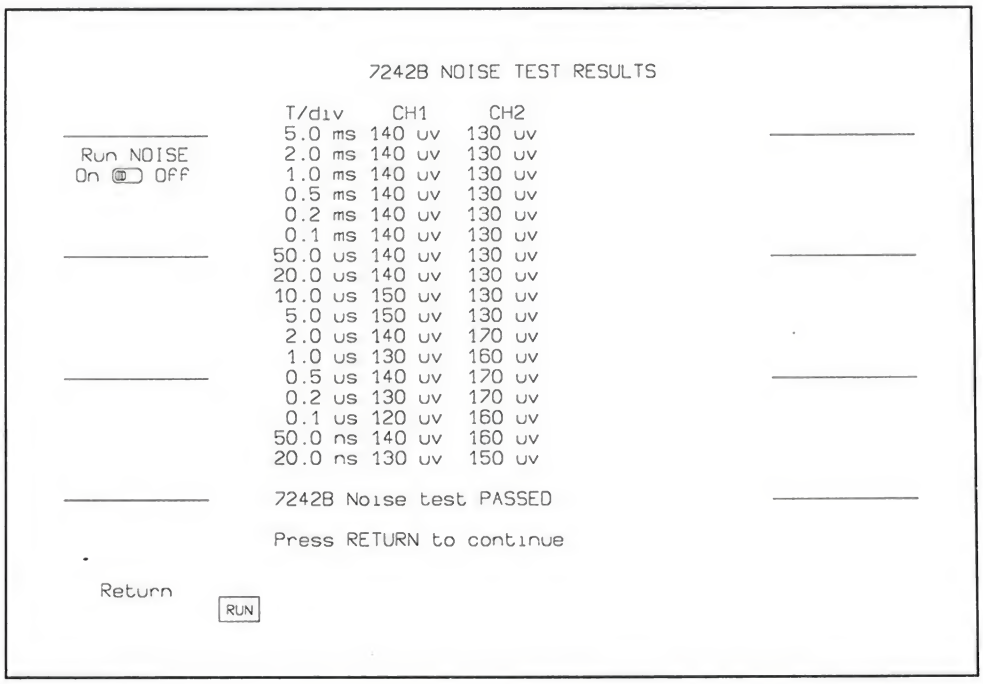


Fig 2.4

2.2.3 ADC Codes Test

The ADC test will check that as the offset voltage is ramped from -3.5 divisions to +3.5 divisions, that the baseline sdev does not exceed 1 mV(sdev) on the 5mV range on all channels. This test will be performed at 1 ns/pt., 2.5 ns/pt. and 5 ns/pt (5ns/pt only on 7234).

- Connect 50Ω terminators to CH1, CH2, CH3, and CH4 inputs.

- If the selected LOG TYPE is either Printer or Floppy then the adc test data will be collected automatically. If NO LOG was selected, when the test is complete the results will be displayed on the screen as in Fig 2.5. Record these results in Table 2.2. Follow the displayed instructions.

  The module controls will be set as follows:

Trace 1:	on :Ch1
Trace 2:	on :Ch2
Trace 3:	on :Ch3 (7234 only)
Trace 4:	on :Ch4 (7234 only)
Grid:	single
Input couplings CH1,CH2,CH3,CH4:	DC
Input gain:	5 mV/div
Time/div:	2,5,10 usec (2 us 7234)

Trigger:

SMART trigger:	off
Source:	Line
Coupling:	AC
Level :	zero
MODE:	auto

Extended parameters are as follows:

T1 : SDEV
T2 : SDEV
T3 : SDEV (7234 only)
T4 : SDEV (7234 only)

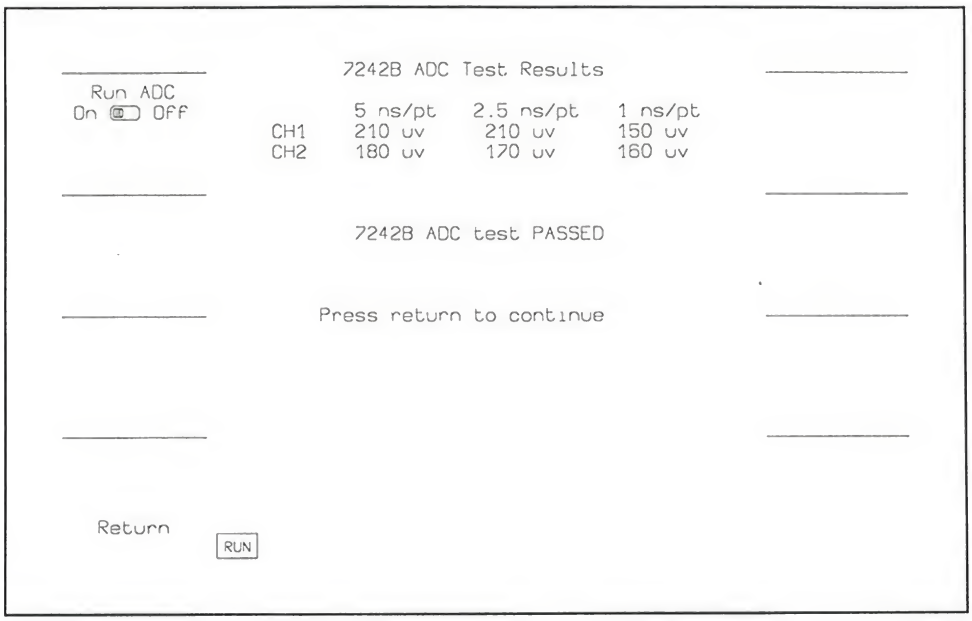


Fig 2.5

2.2.4 DC Gain and Linearity

The DC gain and linearity test will check that the DC accuracy of the module is within 2%. The report generated by the test will display the percent error for each channel and each volts per division setting.

- Connect a precision DC supply, set to 0 v to the channel 1 input. If the selected LOG TYPE is either Printer or Floppy then the DC gain and linearity test data will be collected automatically. If NO LOG was selected, when the test is complete the results will be displayed on the screen as in Fig 2.6. Record these results in Table 2.3. Follow the displayed instructions.

  The module controls will be set as follows:

Trace 1:	on
Grid:	single
Input couplings: Channel under test:	50 ohms DC
Input gain:	5mv/div
Time/div:	0.5ms
Trigger:	
SMART trigger:	off
Source:	Line

Extended parameters are as follows:

T1 : MEAN

- Press RETURN

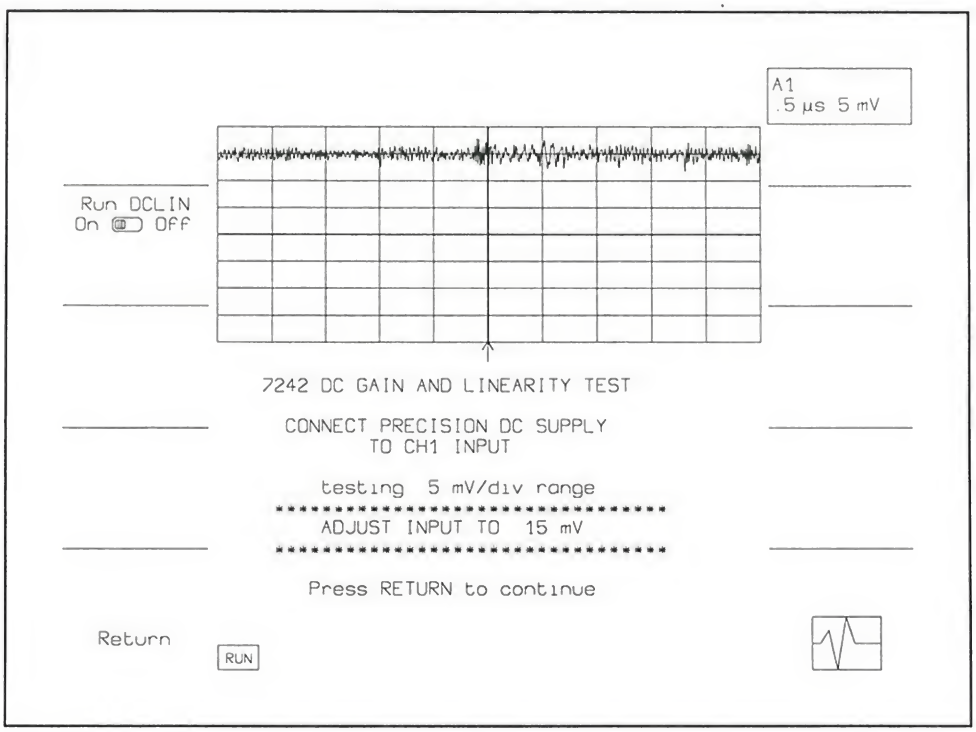


Fig 2.6

- Adjust input to 15mv
- Press RETURN

The 7200 will calculate the average mean value for 100 sweeps of 2000 points each (200,000 points). A menu as in Figure 2.6 will be displayed after each step of the test. The menu will display what voltage range is to be tested next and what voltage and polarity to adjust the DC supply to.

- Adjust the DC supply to the voltage indicated in the menu on the display.
- Press RETURN
- Repeat the above 2 steps until the message in Figure 2.7 is displayed.
- Move the DC supply output to the next channel indicated
- Press RETURN to continue
- Repeat the above 5 steps until a PASS or FAIL message is displayed on the screen.

Pressing RETURN will end the test. If NO LOG was selected, when the test is complete the results will be displayed on the screen as in Fig 2.7. Record these results in table 2.3.

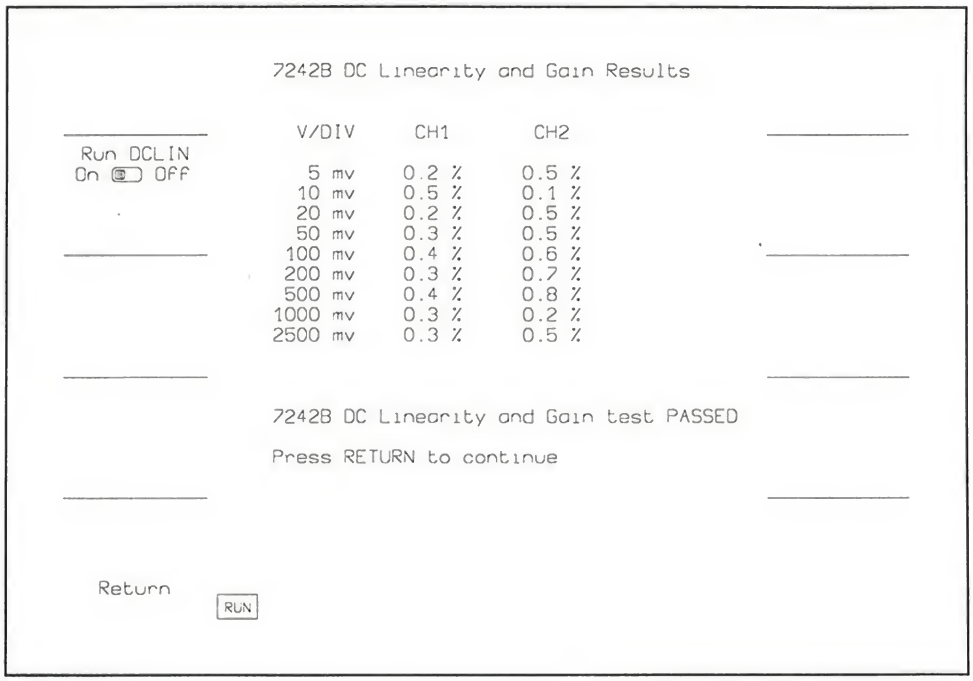


Fig 2.7

2.2.5 Trigger Level Accuracy

The trigger level accuracy test will check that the voltage level of the input signal is within 5% of the range of the trigger level setting, 10% for external trigger. If the selected LOG TYPE is either Printer or Floppy then the trigger accuracy data will be collected automatically. If NO LOG was selected, when the test is complete the results will be displayed on the screen as in Fig 2.8. Record these results in Table 2.4. Follow the displayed instructions.

- Connect a 10 Khz, 250 mv rms sine wave to the channel 1 input.
- Press RETURN

The module controls will be set as follows:

Trace 1:	on
Grid:	single
Input couplings: Channel under test:	50 ohms DC
Input gain:	100mV/div
Time/div:	20 us
Trigger:	
SMART trigger:	off
Source:	Channel under test
Level:	Based on table
Coupling:	DC

RANGE = +/- 5*(v/div) = +/- 5*100mV = +/- 500mv
RESOLUTION = 0.025% of range = 0.00025 * 500mv = 125uV
ACCURACY = +/- 5% of range = +/- 25mv
+/- 10% of range = +/- 50 mv (external input)

If any range was found to be out of the specified accuracy, the measurement will be preceded and followed by asterisks. When the test of CH1 is complete a message will be displayed directing the user the move the input signal to the next channel. Both positive and negative slope trigger will be tested for all trigger inputs. Results outside these limits will be marked failed on the test results.

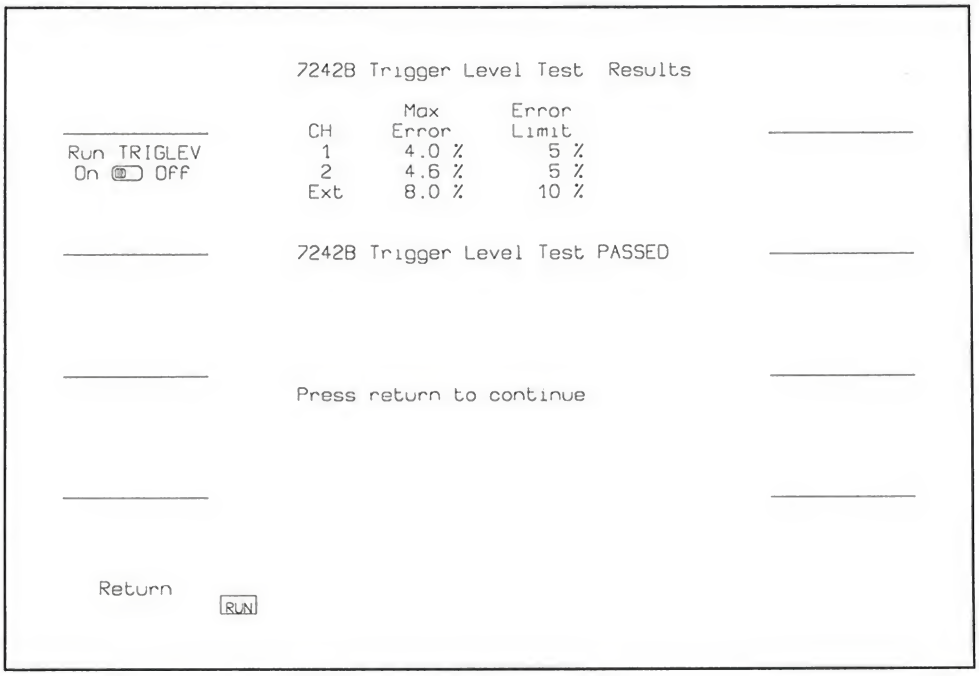


Fig 2.8

- Move the sine wave generator output to the input of the next channel indicated.
- Press RETURN to continue
- Repeat the above 2 steps until a PASS or FAIL message is displayed on the screen.
- If NO LOG was selected, the results will be displayed on the screen. Record these results in table 2.4.

2.2.6 Timebase Accuracy

This test will verify that the timebase is within 0.001% of its stated value.

- In order to verify the time base, use a sine wave generator with a frequency accuracy of better than 1 PPM. If the selected LOG TYPE is either Printer or Floppy then the timebase test data will be collected automatically. If NO LOG was selected, when the test is complete the results will be displayed on the screen as in Fig 2.9. Record these results in Table 2.6. Follow the displayed instructions.

The Panel setting for the Timebase Accuracy Test is:

Input Coupling:	50 Ω DC
Input Gain:	200mv/div
Offset:	ZERO
Time / Div:	0.1 S
RIS:	OFF
Trigger:	Line

Extended Parameters are:
T1: freq

- Connect sine wave generator to CH1 input
- Adjust input frequency to 10 MHz
- Adjust input amplitude to 6 divisions (approx. 225 mv rms)
- Check that T1:freq<100Hz
- The frequency being displayed is the difference (or aliased) frequency between the input signal and the modules sample clock. The test limit is 100Hz(or .001%).
- Record T1:freq on the test results data sheet

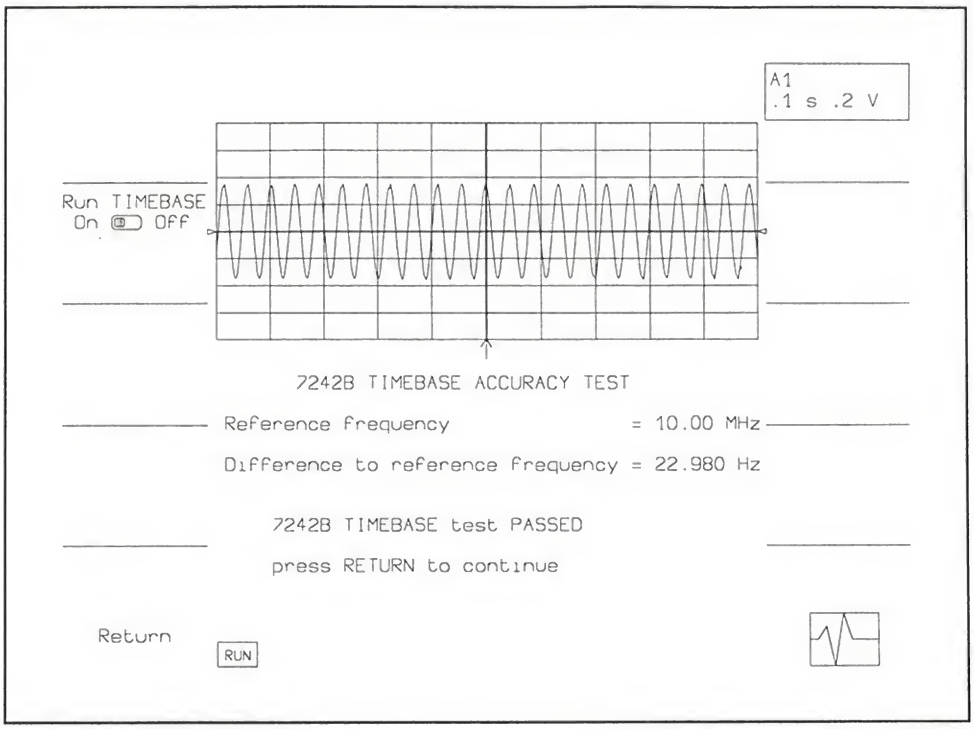


Fig 2.9

2.2.7 Trigger Delay & Front End Test

This test will verify that the trigger point is within 1 nsec of the trigger delay setting. It will also check the overshoot of the input amplifier is less than 10%.

- Connect a 10 Khz, 700 mv p-p square wave with a rise time of less than 1 ns to the channel 1 input. If the selected LOG TYPE is either Printer or Floppy then the trigger delay data will be collected automatically. If NO LOG was selected, when the test is complete the results will be displayed on the screen as in Fig 2.10. Record these results in Table 2.6. Follow the displayed instructions.

  The module controls will be set as follows:

Trace 1:	on
Input couplings CH1 and CH2:	50 Ω DC
Input gain:	200mV/div
Time/div:	2ns
Trigger:	
SMART trigger:	off
Source:	Channel under test
Level:	Based on table
Coupling:	DC

Extended parameters are as follows:

T1:tafl	T1:tars
T1:ampl	T1:freq
T1:ovsp	T1:ovsn

- Press RETURN
- When the test of CH1 is complete a message will be displayed directing the user to move the input signal to the next channel.
- Press RETURN to continue
- Repeat the above 2 steps until a PASS or FAIL message is displayed on the screen.
- If NO LOG was selected the results will be displayed on the screen as in Fig 2.10. Record these results in table 2.6.

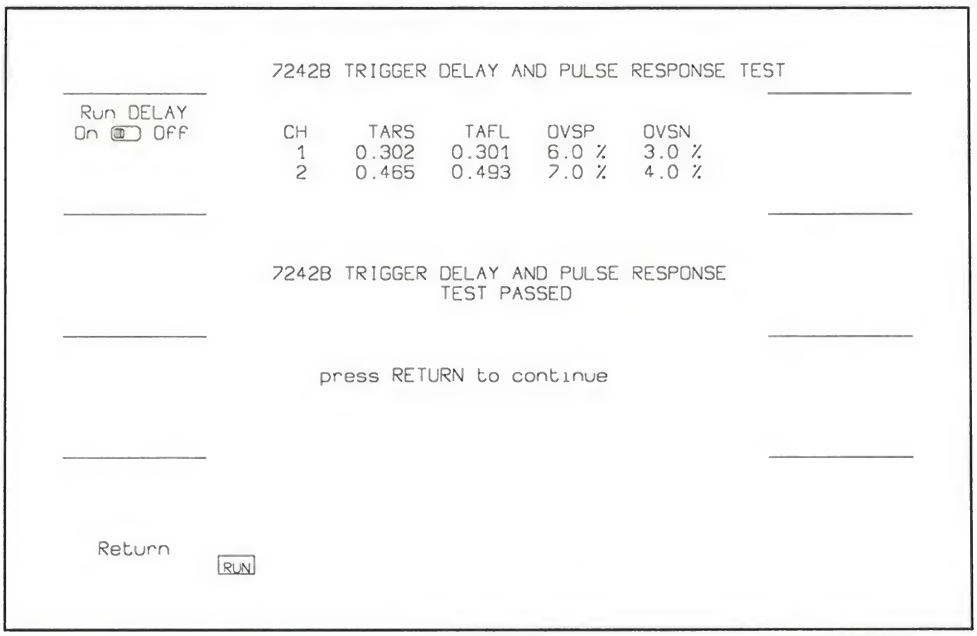


Fig 2.10

2.2.8 Bandwidth

This test will verify that the bandwidth is greater than 400 MHz for a 7242 and 500 MHz for a 7242A, 7242B and 7234. It will also check the flatness of the frequency response.

- Connect a leveled sine wave generator to the channel 1 input*. If the selected LOG TYPE is either Printer or Floppy then the bandwidth data will be collected automatically. If NO LOG was selected, when the test is complete the results will be displayed on the screen as in Fig 2.11. Record these results in Table 2.7. Follow the displayed instructions.

  The module controls will be set as follows:

Trace 1:	on
Grid:	single
Input couplings CH1 and CH2:	50 Ω DC
Input gain:	50mV/div
Time/div:	2.5 us
Trigger:	
SMART trigger:	off
Source:	Line

Extended parameters are as follows:

T1:rms

- Adjust amplitude of generator to 100 mv rms * correction factor. (If no correction factor is available use 1.0, however unit may fail BW test if loss in cable is to great or generator output is not flat.
- Press RETURN

---

* To verify the flatness of the generator and cable, measure the loss of the cable used to measure the bandwidth of the system. Apply a 2MHz -7.1db signal to the cable. Measure the amplitude at the output of the cable, with a calibrated power meter, press the relative button. Now change the frequency to 401 and 501MHz and measure the amplitude again, the display will read the difference. Calculate the correction factor as follows:

correction factor = 10E-Difference/20

For example, if the difference is -.3db then

correction factor = 10E.3/20 = 10E.015 = 1.035

Record this correction factor, the difference in db, and the serial number of the signal generator on a card attached to the cable.

- A message will be displayed directing the user to increase the input signal's frequency until the maximum frequency for that module is reached. The signal will be aliased when the frequency is greater than 101 MHz.
- When the test of CH1 is complete a message will be displayed directing the user to move the input signal to the next channel.
- Press RETURN to continue
- Repeat the above 2 steps until a PASS or FAIL message is displayed on the screen.
- If NO LOG was selected the results will be displayed on the screen as in Fig 2.10. Record these results in table 2.6.

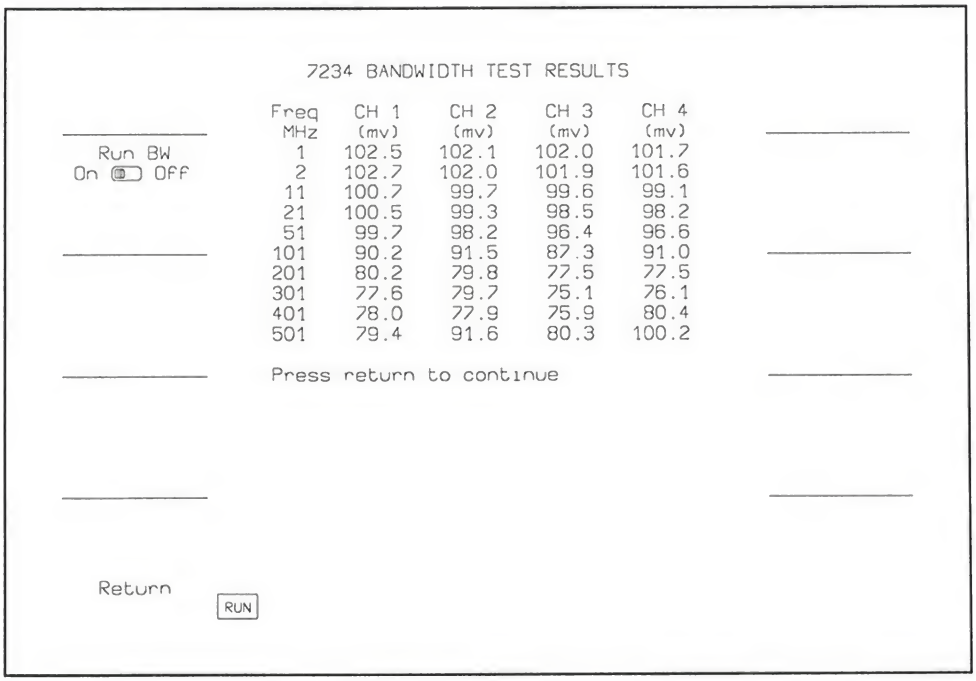


Fig 2.11

2.2.9 Input Impedance

- Using a DVM with accuracy better than 0.1 Ω :
- Connect DVM to BNC input of channel under test
- Check the input impedance for all gain ranges and input couplings listed in table 2.7 and record the measured impedance on the test results work sheet: (change gain range by turning V/DIV knob)
- Change input coupling to DC 1 MΩ and repeat above tests

The limits for the 1 Meg ohm input impedance test are between 980,000 ohms and 1,020,000 ohms, the limits for 50 ohm input impedance are 49 ohms and 51 ohms.

DATA SHEET : Baseline Noise

V/div	Time/div	CH 1 (limit 1.0 mV)	CH 2 (limit 1.0 mV)	CH 3 (limit 1.0 mV)	CH 4 (limit 1.0 mV)
5 mV	5 msec				
	2 msec				
	1 msec				
	0.5 msec				
	0.2 msec				
	0.1 msec				
	50 usec				
	20 usec				
	10 usec				
	5 usec				
	2 usec				
	1 usec				
	0.5 usec				
	0.2 usec				
	0.1 usec				
	50 nsec				
	20 nsec				

Mainframe Serial Number	Plug-in Serial Number	TEST DATE	PERFORMED BY

Table 2.1

DATA SHEET : ADC test

V/div	Channel	5 ns/pt	2.5 ns/pt	1 ns/pt
5 mV	1			
	2			
	3			
	4			

Mainframe Serial Number	Plug-in Serial Number	TEST DATE	PERFORMED BY

Table 2.2

DATA SHEET : DC Gain and Linearity

Limit < 2% error

V/div	DC Input	CH1	CH2	CH3	CH4
5 mV	±15 mV				
10 mv	±30 mV				
20 mv	±60 mV				
50 mv	±150 mv				
100 mv	±300 mv				
200 mv	±600 mv				
500 mv	±1500 mv				
1 v	±1500 mv				
2.5 v	±1500 mv				

Mainframe Serial Number	Plug-in Serial Number	**TEST DATE**	**PERFORMED BY**

Equipment Used : Mfg, Model Number	Calibration Information

Table 2.3

DATA SHEET : Trigger Level Accuracy

Channel	Max Error	Error Limit
1		5 %
2		5 %
3		5 %
Ext		10 %

Mainframe Serial Number	Plug-in Serial Number	TEST DATE	PERFORMED BY

Equipment Used : Mfg, Model Number	Calibration Information

Table 2.4

DATA SHEET : Timebase

	CH1 (Hz)
FREQ (limit < 100)	

Mainframe Serial Number	Plug-in Serial Number	**TEST DATE**	**PERFORMED BY**

Equipment Used : Mfg, Model Number	Calibration Information

Table 2.5

DATA SHEET : Trigger Delay and Pulse Response

	CH 1	CH 2	CH 3	CH 4
TARS (limit < 1 ns)				
TAFL (limit < 1 ns)				
OVSP (limit < 10 %)				
OVSN (limit < 10 %)				

Mainframe Serial Number	Plug-in Serial Number	**TEST DATE**	**PERFORMED BY**

Equipment Used : Mfg, Model Number	Calibration Information

Table 2.6

2.2.10 DATA SHEET : Bandwidth

Test assumes flat response from generator and no losses in cable from generator to input of module unless correction factor is used. Check box below and indicate correction factor if correction factor is being used. Input signal amplitude is 100 mv rms * correction factor.

Correction factor used to adjust input signal amplitude_____.

Input Freq. (MHz)	CH 1 (mv rms)	CH 2 (mv rms)	CH 3 (mv rms)	CH 4 (mv rms)	Limit (mv rms) 7242 only	Limit (mv rms) 7242A/B 7234
6					≥ 100	≥ 100
251					≥ 74	≥ 74
301					≥ 72	≥ 74
401					≥ 70.7	≥ 72
501					N/A	≥ 70.7

Mainframe Serial Number	Plug-in Serial Number	**TEST DATE**	**PERFORMED BY**

Equipment Used : Mfg, Model Number	Calibration Information

Table 2.7

DATA SHEET : Input Impedance

	Input Coupling	CH 1	CH 2	CH 3	CH 4	Limit
5 mv	50 Ω					49 - 51 Ω
10 mv	50 Ω					
20 mv	50 Ω					
50 mv	50 Ω					
100 mv	50 Ω					
200 mv	50 Ω					
500 mv	50 Ω					
1 v	50 Ω					
5 mv	DC 1 MΩ					980 K - 1.02 MΩ
10 mv	DC 1 MΩ					
20 mv	DC 1 MΩ					
50 mv	DC 1 MΩ					
100 mv	DC 1 MΩ					
200 mv	DC 1 MΩ					
500 mv	DC 1 MΩ					
1 v	DC 1 MΩ					

Mainframe Serial Number	Plug-in Serial Number	**TEST DATE**	**PERFORMED BY**

Equipment Used : Mfg, Model Number	Calibration Information

Table 2.8

2.3 7262 NIST CALIBRATION PROCEDURE

2.3.1 Setup

Place the 7262 under test in slot A.

Execute default settings on the 7200 series mainframe.

Load and Run ICL program "NIST" located on "7200A NIST DATA" disk.

Select Data Logging type. Choose Either "Log Printer" or "Log Floppy" or "No Log"

Press RETURN.

NOTE: For each of the following tests if a specification limit is exceeded mark the failed range with an ASTERISK .

2.3.2 BaseLine Noise

The NOISE test will check that the baseline noise does not exceed 0.6 mV (sdev) on the 10 V/div range and 5.0 mV (sdev) on the 100 mV/div range for both channels. This test will be performed at selected timebase ranges between 20 usec - 20 nsec.

Enter the serial number of the 7262 under test and today's date on the data sheet.
Connect 50 terminators to CH1, and CH2 inputs.
If selected LOG TYPE is either Printer or Floppy then:

- Press "NOISE62"
- The Noise data will be collected automatically. Follow the displayed instructions. Proceed to Trigger Level Accuracy test.

Otherwise:

- Press "RETURN"
- Follow the remaining steps.

Set the 7262 controls as follows:

Trace 1:	on : A1
Trace 2:	on : A2
Grid:	single
Input couplings CH1 and CH2:	DC
Input gain:	10 mV/div
Time/div:	20 usec
Trigger:	
SMART trigger:	off
Source:	CH1
Coupling:	DC
Level :	zero
MODE:	auto

Extended parameters are as follows:
T1 : SDEV
T2 : SDEV

Using the data sheet as a guide switch through all time/div settings listed and record SDEV for both channels.

DATA SHEET : Baseline Noise

V/div	Time/div	CH 1 (limit 0.6 mV)	CH 2 (limit 0.6 mV)
10 mV	20 usec		
	5 usec		
	2 usec		
	.5 usec		
	.1 usec		
	50 nsec		
	20 nsec		
V/div	**T/div**	**CH 1 (limit 5.0 mV)**	**CH 2 (limit 5.0 mV)**
100 mV	20 usec		
	5 usec		
	2 usec		
	.5 usec		
	.1 usec		
	50 nsec		
	20 nsec		

Mainframe Serial Number	Plug-in Serial Number	TEST DATE	PERFORMED BY

2.3.3 Trigger Level Accuracy

This test verify the accuracy of the trigger level circuit. The test will be performed at the 10 mV/div and 100 mv/div ranges. The test limits are based on the following criteria:

RANGE = ± 80 mV (10 mV/div) ; ± 800 mV (100 mV/div)
RESOLUTION = 2% of full scale
ACCURACY = +/- 5% of full scale

Connect a sinewave generator to CH1
Adjust input frequency to 100 KHz, adjust input amplitude to 80 mVp-p
If selected LOG TYPE is either Printer or Floppy then:

- Load and run ICL program "TRIGLV62"
  - The data will be collected automatically. Follow the displayed instructions. Proceed to DC Gain and Linearity test.

Otherwise:

- Press "RETURN"
- Follow the remaining steps.

Enter the serial number of the 7262 under test and today's date on the data sheet.
Press "PANEL SETUP".
Recall "TRGLEV62" from the floppy.
Press "RETURN"
Verify the 7262 controls as follows:

Trace 1:	on : A1
Trace 2:	on : A2
Grid:	single
Input couplings CH1 and CH2:	DC
Input gain:	10 mV/div
Time/div:	5 nsec
Vertical:	AVG ON
Trigger:	
SMART trigger:	off
Source:	CH1
Coupling:	DC
Polarity:	POS
Level:	zero
MODE:	normal

Extended parameters are as follows:

T1 : MEAN T2 : MEAN

Measure the mean value at the trigger point for both positive and negative trigger polarity and record the results on the data sheet.
Complete the data sheet.

NOTE: For 100 mV/div set sinewave generator to 800 mV_{pp}

DATA SHEET : Trigger Level Accuracy

V/div	Trig Level	CH1 POS	CH1 NEG	CH2 POS	CH2 NEG	Limits (mV)
10 mV	0 V					-4 to 4
	8 mV					4 to 12
	- 8 mV					-4 to -12
	16 mV					12 to 20
	- 16 mV					-12 to -20
	32 mV					36 to 28
	-32 mV					-36 to -28
100 mV	0 V					-40 to 40
	80 mV					40 to 120
	-80 mV					-40 to -120
	160 mV					120 to 200
	-160 mV					-120 to -200
	320 mV					280 to 360
	-320 mV					-280 to -360

Mainframe Serial Number	Plug-in Serial Number	**TEST DATE**	**PERFORMED BY**

Equipment Used : Mfg, Model Number	Calibration Information

2.3.4 DC Gain and Linearity

This test verifies DC gain. The test will be performed at the 10 mV/div and 100 mV/div ranges. The test limits are based on the following criteria:

GAIN ACCURACY = ± 3% of full scale
OFFSET ACCURACY = ± 3% of value + 1 mV

If selected LOG TYPE is either Printer or Floppy then:

- Load and run ICL program "DC_LIN62"
- The data will be collected automatically. Follow the displayed instructions. Proceed to Trigger Delay test.

Otherwise:

- Press "RETURN"
- Follow the remaing steps.

Enter the serial number of the 7262 under test and today's date on the data sheet.
Press "PANEL SETUP".
Recall "DCGAIN62" from the floppy.
Press "RETURN"
Verify the 7262 controls as follows:

Trace 1:	on: AVGS A1 (100 sweeps)
Trace 2:	on: AVGS A2 (100 sweeps)
Grid:	single
Input couplings CH1 and CH2:	DC
Input gain:	10 mV/div
Time/div:	1 usec
Trigger:	
SMART trigger:	off
Source:	PULSE
Coupling:	DC
Level:	zero
MODE:	auto

Extended parameters for CH1 are as follows:

T1 : MEAN T2 : MEAN

Connect a precision DC supply to CH1 or CH2 inputs.
Adjust input to 10 mV
Press CLEAR DISPLAY

NOTE: The 7200 will now calculate the MEAN value for 100 sweeps.

Record the results on the data sheet.
Using the data sheet as a guide adjust the V/div setting, Input offset and input DC level and complete the test.

DATA SHEET : DC Gain and Linearity

V/div	Offset	DC Input	CH1	CH2	Limit (mV)
10 mV	0 V	10 mV			6.6 to 13.4
	0 V	-10 mV			-6.6 to -13.4
	0 V	20 mV			16.6 to 23.4
	0 V	-20 mV			-16.6 to -23.4
	0 V	30 mV			26.6 to 33.4
	0 V	-30 mV			-26.6 to -33.4
	80 mV	-110mV			-104.2 to -115.8
	-80 mV	110 mV			104.2 to 115.8
100 mV	0 V	100 mV			66 to 134
	0 V	-100 mV			-66 to -134
	0 V	200 mV			166 to 234
	0 V	-200 mV			-166 to -234
	0 V	300 mV			266 to 334
	0 V	-300 mV			-266 to -334
	800mV	-1.1 V			-1.051 to -1.149
	-800mV	1.1 V			1.051 to 1.149

Mainframe Serial Number	Plug-in Serial Number	TEST DATE	PERFORMED BY

Equipment Used : Mfg, Model Number	Calibration Information

2.3.5 Trigger Delay

Enter the serial number of the 7262 under test and today's date on the data sheet.
Press "PANEL SETUP".
Recall "Delay62" from the floppy.
Press "RETURN"
Verify the 7262 controls as follows:

Trace 1:	on : A1
Trace 2:	on : A2
Grid:	single
Input couplings CH1 and CH2:	DC
Input gain:	200 mV/div
Time/div:	2 nsec

Trigger:

SMART trigger:	off
Source:	CH1
Slope:	positive
Coupling:	DC
Level:	zero
MODE:	auto

Extended parameters are as follows:

T1:TAFL	T2:TAFL
T1:TARS	T2:TARS

Connect a square wave generator with a risetime of better than 1 nsec to CH1 input and adjust input amplitude to 600 mVp-p with 0 volt DC offset. Adjust the frequency to 40 Mhz.
Record CH1 "TARS" on the data sheet.
Change trigger slope to negative
Record CH1 "TAFL" on the data sheet.
Connect the input to channel 2 and repeat the previous steps.

DATA SHEET : Trigger Delay

	CH 1 (limit 500 psec)	CH 2 (limit 500 psec)
TARS		
TAFL		

Mainframe Serial Number	Plug-in Serial Number	**TEST DATE**	**PERFORMED BY**

Equipment Used : Mfg, Model Number	Calibration Information

2.3.6 Time Base Accuracy

Enter the serial number of the 7262 under test and today's date on the data sheet.
Press "CONFIG SYSTEM".
Press "PANEL SETUP".
Recall "Times62" from the floppy.
Press "RETURN"
Verify the 7262 controls as follows:

Trace 1:	on
Grid:	single
Input couplings CH1 and CH2:	DC
Input gain:	100 mV/div
Time/div:	100 ms
Trigger:	
SMART trigger:	off
Source:	CH1
Coupling:	DC
Level:	zero
MODE:	auto

Extended parameters are as follows:
T1 : FREQ

NOTE: *In order to verify the time base, use a sine wave generator with a frequency accuracy of better than 1 ppm.*

Connect sine wave generator to CH1 input
Adjust input frequency to 10 Mhz
Adjust input amplitude to 6 divisions.
Check that T1:freq<100Hz The frequency being displayed is the difference (or aliased) frequency between the input signal and the plug-in's sample clock. The test limit is 100Hz (or .001%).
Record the test results on the data sheet.

DATA SHEET : Time Base Accuracy

	CH 1 (limit < 100 Hz)
FREQ	

Mainframe Serial Number	Plug-in Serial Number	**TEST DATE**	**PERFORMED BY**

Equipment Used : Mfg, Model Number	Calibration Information

2.3.7 Input Impedance

Enter the serial number of the 7262 under test and today's date on the data sheet.
Press "CONFIG SYSTEM".
Press "PANEL SETUP".
Recall "IMED62" from the floppy.
Press "RETURN"
Verify the 7262 controls as follows:

Trace 1:	on:
Trace 2:	on:
Grid:	single
Input couplings CH1 and CH2:	DC
Input gain:	10 mV/div
Time/div:	0.5 ms
Trigger:	
SMART trigger:	off
Source:	CH1
Coupling:	DC
Level:	zero
MODE:	auto

Connect DVM to CH 1
Calibrate the 7262.
Check the 50 ohm input impedance for all gain ranges and record the measured impedance on the data sheet.

Note: The limits for the 50 ohm input impedance test are between 49.5 ohms and 50.5 ohms.

DATA SHEET : Input Impedance

V/div	CH 1 (limit 49.5 to 50.5)	CH 2 (limit 49.5 to 50.5)
10 mV		
100 mV		

Mainframe Serial Number	Plug-in Serial Number	TEST DATE	PERFORMED BY

Equipment Used : Mfg, Model Number	Calibration Information

2.3.8 Front End

Enter the serial number of the 7262 under test and today's date on the data sheet.
Press "CONFIG SYSTEM".
Press "PANEL SETUP".
Recall "OVER62" from the floppy.
Press "RETURN"
Verify the 7262 controls as follows:

Trace 1 , 2	on, T2 Hampl(A1)
Trace 3 , 4	on, T4 Hampl(A2)
Grid:	Dual
Input couplings CH1 and CH2:	DC
Input gain:	5 mV/div
Offset: (CH1 & CH2)	-20 mV
Time/div:	0.5 nsec
Average:	ON
Trigger:	
SMART trigger:	off
Source:	EXT
Polarity:	POS
Coupling:	DC
Level (EXT):	400 mV
MODE:	norm

Extended parameters are as follows:

T2 : RISE	T4 : RISE
T2 : OVSP	T4 : OVSP

Connect the PICO SECONDS PULSE LABS TD-1110C pulse generator with a falltime < 45 psec to CH1 through a 20 dB attenuator. Connect the pulse generator reference output to the 7262 external trigger.
Record the values for CH1 and CH2 of "RISE", and "OVSP" on the data sheet.
Adjust input gain to 50 mV/div, the Offset to -200 mV and remove the 20 dB attenuator.
Record the values for CH1 and CH2 of "RISE", and "OVSP" on the data sheet.

DATA SHEET : Front End

V/div		LIMITS	CH 1	CH 2
5 mV	RISE	< 155 psec		
	OVSP	< 12 %		
50 mV	RISE	< 130 psec		
	OVSP	< 10 %		

Mainframe Serial Number	Plug-in Serial Number	TEST DATE	PERFORMED BY

Equipment Used : Mfg, Model Number	Calibration Information

ADJUSTMENTS

3.0 INTRODUCTION

This section includes the adjustments required for the instrument. It is recommended that the calibration be verified at one year intervals.

NOTE:

These calibrations are included in this manual for completeness but are only intended for use by factory authorized service centers. Many of the test programs and adjustments required are not accessible without specialized test fixtures or software keys.

3.1 DELAY CALIBRATION

1) Connect "dongle"[1] to parallel port on rear of mainframe.
2) Insert appropriate delay cal disk into floppy drive.
3) Press Modify and then Run Program .
4) Select:

Speed	Fast
Disk	Floppy
Recall filename	Startup

5) Press Recall, Return and then Run Startup.
6) Follow the directions on the screen until screen display PASS.
7) Remove floppy disk from system and cycle power.

3.2 ADC TIMING CALIBRATION

1) Input a 100 MHz 90% full scale sine wave into both channels.
2) Adjust VARDLY2 to the right on the ADCA board until flyers are first noted on either channel. Note where the slider is set. Adjust VARDLY2 to the left and note where the slider is when fliers are first observed. Set the slider to the midpoint of these two settings.
3) Adjust VARDLY4 on the ADCA in the same manner as step 2.
4) Readjust VARDLY2 as in step 2.

[1] A dongle is a software key which plugs into the parallel port and enables the system test environment.

3.3 ADC TRACK AND HOLD OFFSET CALIBRATION

1) Remove the 10 MHz reference clock from the reference input of the ADCA card and put it on the external clock input of the ADCA card if the ADCA is on a 1712 ADCA test icon or input a 10 MHz external clock. Select external clock from the Modify Timebase menu. Set the timebase to 1 Ns/point. Disconnect all inputs to the amplifier and set the offset to zero.

2) On an HMS603 or HMS603A probe the small gold tabs on the substrate of the hybrid on the end opposite the input signal with a high impedance analog scope. Ground the probe and set the analog scope to 20 MHz bandwidth limit and maximum sensitivity on the volts per division range. On an HMS403B disconnect the SMB connector from the AMP and connect a cable from the analog scope to the input SMB on the ADCA card.

3) Referring to table 5.3 adjust the appropriate pot while probing the correct tab on the HMS603(A) so the offset is 0 v.

Channel	Flash	Pot	HMS603 (A) U#	Tab to probe on HMS603A	SMB to probe on HMS403B
1	A	R130	U3	Front	CH1
1	B	R133	U3	Rear	CH1
1	C	R136	U3	Front	CH1
1	D	R139	U3	Rear	CH1
2	A	R306	U16	Front	CH2
2	B	R310	U16	Rear	CH2
2	C	R314	U16	Front	CH2
2	D	R318	U16	Rear	CH2

Table 3.3

3.4 EXTERNAL CLOCK CALIBRATION

1) Place the ADCA board onto a 7242(A/B) module with a 1712 ADC test icon fitted.

2) Input a 1 GHz sine wave at -3dbm into the external clock input. Select external clock from the modify timebase menu. Connect a 350 MHz scope to the SMB clock test point.

3) Adjust R566 until you see the 250 MHz clock at the SMB test point. It should be a 250 MHz square wave (4 nsec period). Disconnect the external clock and turn R566 until the clock stops. Connect the clock once more to verify it turns on again.

4) Connect a 7291 to the amplifier and input a 45 MHz 80% amplitude sine wave. Press Modify and Cursor Measurements. Add a parameter for channel 1 and 2 of SEBT, set frequency argument to 0 MHz. Set timebase to 100 Ns/div., channel 1 and 2 to 20 mv/div., memory size to 10K and offset to 0 V.

5) Adjust R569 for the best sinefit. It should be greater than 6 effective bits.

3.5 TMB CAL DAC CALIBRATION

1) Place the TMB board onto a 7242(A/B) module with a 1711 TMB test icon fitted. Connect a 7242AMP to TMB.
2) Press configure system, system test.
3) Select :

Disk	Floppy
Module	P42 for a 7242TMB
	P34 for a 7234TMB
Test	TESTTMB
Interactive	YES
Iterations	1

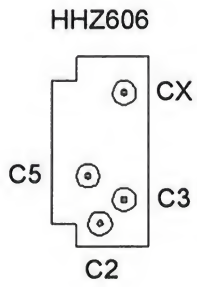
4) Press execute.
5) Following the directions on screen, step through the program until TRIM DAC appears. Follow the directions and adjust R108 and R139 on a 7234TMB and R131 and R148 on a 7242TMB.

3.6 EXTERNAL TRIGGER OFFSET CALIBRATION

1) Remove shields from EXTR.
2) Place plugin in slot A of mainframe and turn on power switch.
3) Set channel 1 to .2 v/div. 50 Ω coupling.
3) Connect a 10 KHz sine wave with a "Tee" at the EXT. input terminate at channel 1.
4) Set trigger source to EXT, trigger coupling to DC, trigger level 0 V and trigger delay 0 ns (50%).
5) Switching the slope back and forth between POS and NEG adjust R4 so the distance between the trigger point and the centerline is equal for both slopes.
6) Reinstall shields on EXTR.

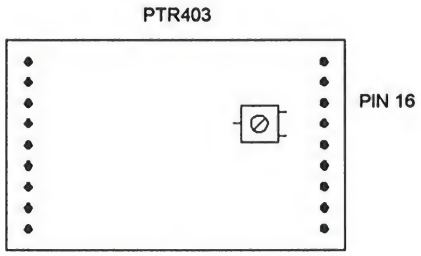
3.7 High Imedance Amplifier (HHZ606) Calibration

1) Extended AMP from TMB using ribbon cables.
2) Set input coupling to DC 1 Mohm.
3) Set gain range to 50 mv/div.
4) Set offset to 0V.
5) Set trigger source to be the channel under test.
6) Set trigger level to 0V.
7) Set timebase to 20 us/div
8) Connect a 10 Khz 150 mv p-p square wave with a 50 Ohm terminator to the channel under test.
9) Refer to the diagram below and adjust C2 for the flatest top of the square wave.
10) Change gain range to 500 mv/div.
11) Adjust square wave amplitude to 1.5V.
12) Adjust C3 for no overshoot and C5 for flattest top'
13) Change gain range back to 50 mv/div.
14) Readjust square wave amplitude back to 150 mv p-p.
15) Readjust C2 for the flatest top of the square wave.
16) Connect BNC cable to sine wave generator.
17) At other end of cable attach a BNC "Tee" with a 50 Ohm terminator.
18) Using the BNC adapter that comes with a 7200-P12 probe kit, attach the probe tip to the free end on the "Tee"
19) Attach other end of probe to channel under test.
20) Add extended parameter for the channel under test to pk-pk.
21) Set channel under test to 20 mv/div.
22) Set sine wave generator for 1 Mhz and adjust amplitude for 100 mv p-p.
23) Increase amplitude to 250 Mhz and adjust cap CX for > 70.7 mv.



3.8 Trigger Hysteresis (PTR403) Calibration

1. Extended AMP from TMB using ribbon cables.
2. Set input coupling of channel under test to DC 1 Mohm.
3. Set input coupling of other channel to DC 50 Ohm.
4. Set gain range to 100 mv/div.
5. Set offset to 0V.
6. Set trigger source to be the channel under test.
7. Set trigger slope to POS
8. Set timebase to 20 us/div
9. Turn extended parameter on set to PK-PK.
10. Connect hysteresis probe to channel under test with "Tee" and terminate at other channel. Hystersis probe is made from a 464 Ohm resistor (168-531-361) with a .1 uf cap (106-438-104) to ground.
11. Probe pin 16 of PTR403 and adjust trigger level to point in center of range where trace on screen begins to oscillate. (approximately - 130mv)
12. Refer to the diagram below and adjust pot for pk-pk of 38-41 mv. wave.



7242 BASIC OPERATION

4.0 GENERAL DESCRIPTION

4.1 BLOCK DIAGRAM

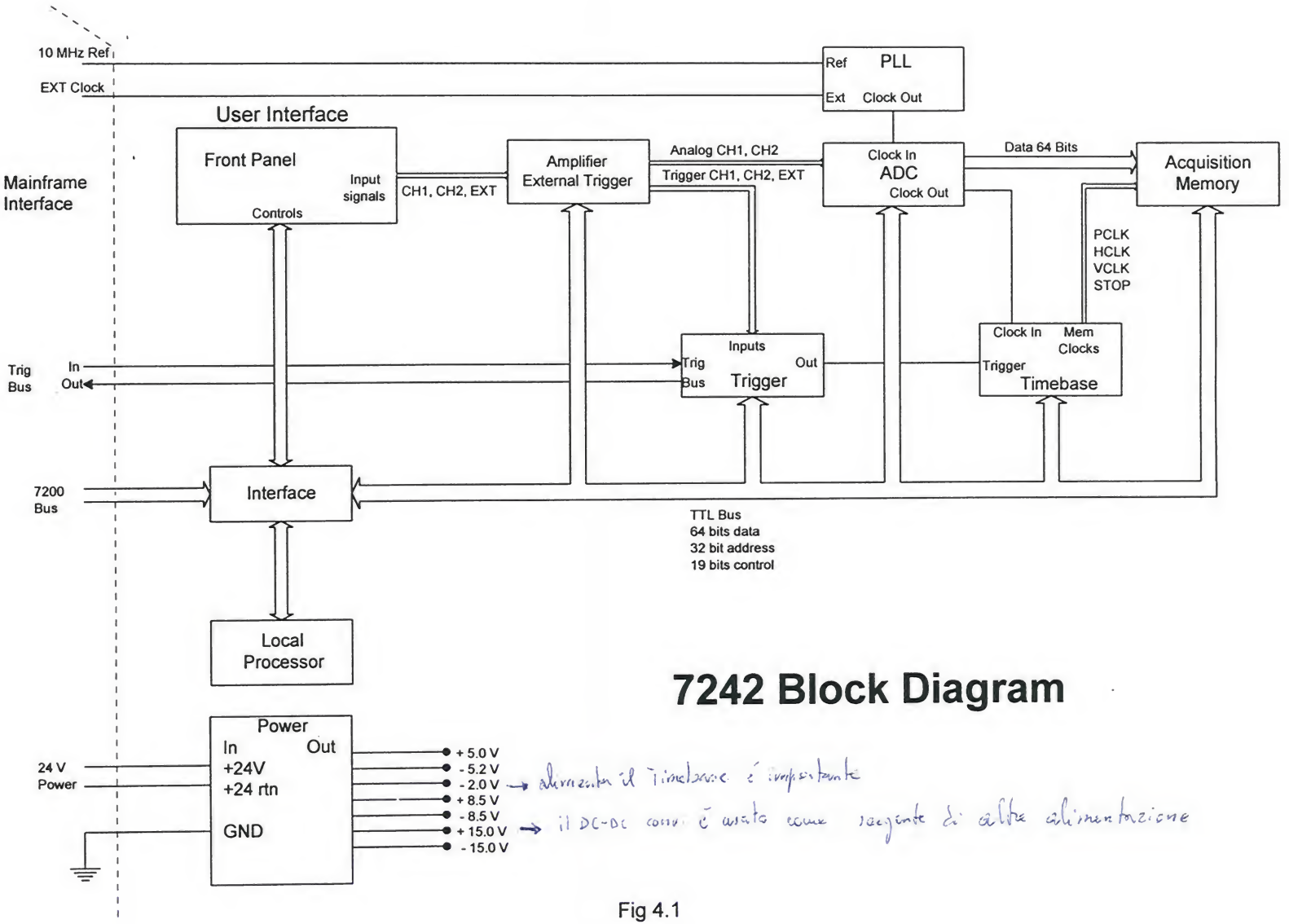
Figure 4.1 is a functional block diagram of the 7242 plug-in, it describes the major functional blocks of the plug-in. The plug-in has two interfaces. One through the 7200 mainframe connectors. The other is the user's interface, the front panel. The mainframe connectors provide power, trigger bus, 10 MHz reference, external sampling clock, and communication between the plug-in and mainframe. Power is provided by a 24 V. supply using three contacts, 24V., 24V. rtn, and GND. The trigger bus allows one plug-in to provide the trigger for other plug-ins in the 7200 system. The 10 MHz reference keeps the sampling frequencies of different plugins in sync. The external sampling clock allows the user to select a different sample clock. The communication between the plug-in and mainframe is over a 96 pin VME style interface.
The ten major blocks in figure 4.1 are:

FRONT PANEL is the user interface. The front panel has four BNC inputs for signals, knobs, buttons and LED's. The controls on the front panel are sufficient to allow basic operation of the plug-in. More complex operations like SMART TRIGGER or waveform math are controlled by menu screens on the 7200 mainframe display.

AMPLIFIER contains two channels of input signal conditioning and their control circuits. Also, the amplifiers generate trigger signals for three of the input signals. The two conditioned analog signals are passed to the ADC and the trigger signals are passed to the trigger block.

TRIGGER selects the module trigger source. The trigger source is selected from one of three input signals, trigger bus (another plug-in), line, or a combination of three input signals using SMART TRIGGER. The timebase uses the selected trigger to stop the acquisition.

ADC converts the two analog signals into two 1 Gsa/s digital signals. The digital signals are 8 bits wide producing a 32 bit data word for the acquisition memory. The PLL provides the 250 MHz and 200 MHz clock for the ADC which is then passed to the timebase.



7242 Block Diagram

Fig 4.1

PLL generates the ADC sampling clock and synchronizes it to the 10 MHz reference of the mainframe. When selected the PLL also enables the external clock and disables the internal clock.

ACQUISITION MEMORY stores the ADC data at a rate of up to 250 Msa/s. The samples are portioned in such a way that when the ADC is only digitizing with one or two flashes the entire memory is available.

TIMEBASE controls various acquisition parameters. The timebase sets the sample rate by decimating the data as it is clocked into the acquisition memory. It controls the acquisition memory addressing via base address and size. It waits the selected trigger delay after the stop trigger is received from the trigger block.

INTERFACE allows the 7200 or the local processor to access the various plug-in control registers.

LOCAL PROCESSOR controls sequence and RIS acquisitions. Also the local processor reorders, corrects, and compacts the plug-in data to produce the display data. This relieves the 7200 processor of this burden to increases the system display update rate as more plug-ins are added to the system.

POWER converters take as input the 24 Volts supplied by the mainframe and produce the supplies used by the subassemblies within the plug-in.

4.2 SUBASSEMBLIES

Figure 5.3 is a connection diagram for the 7242B plug-in, it displays the subassemblies of the 7242B and their interconnections. Figure 5.1 shows how the 7242B is assembled. The subassemblies included in this drawing are:

4.2.1 7242ADCA SUBASSEMBLY

The 7242ADCA is a 1 Gsa/s 2-channel digitizer utilizing 8-bit flash ADC technology. Four 8-bit flashes are dedicated for each channel (see Fig 4.2) . The support circuitry for each channel is identical, each consisting of six major functional components.

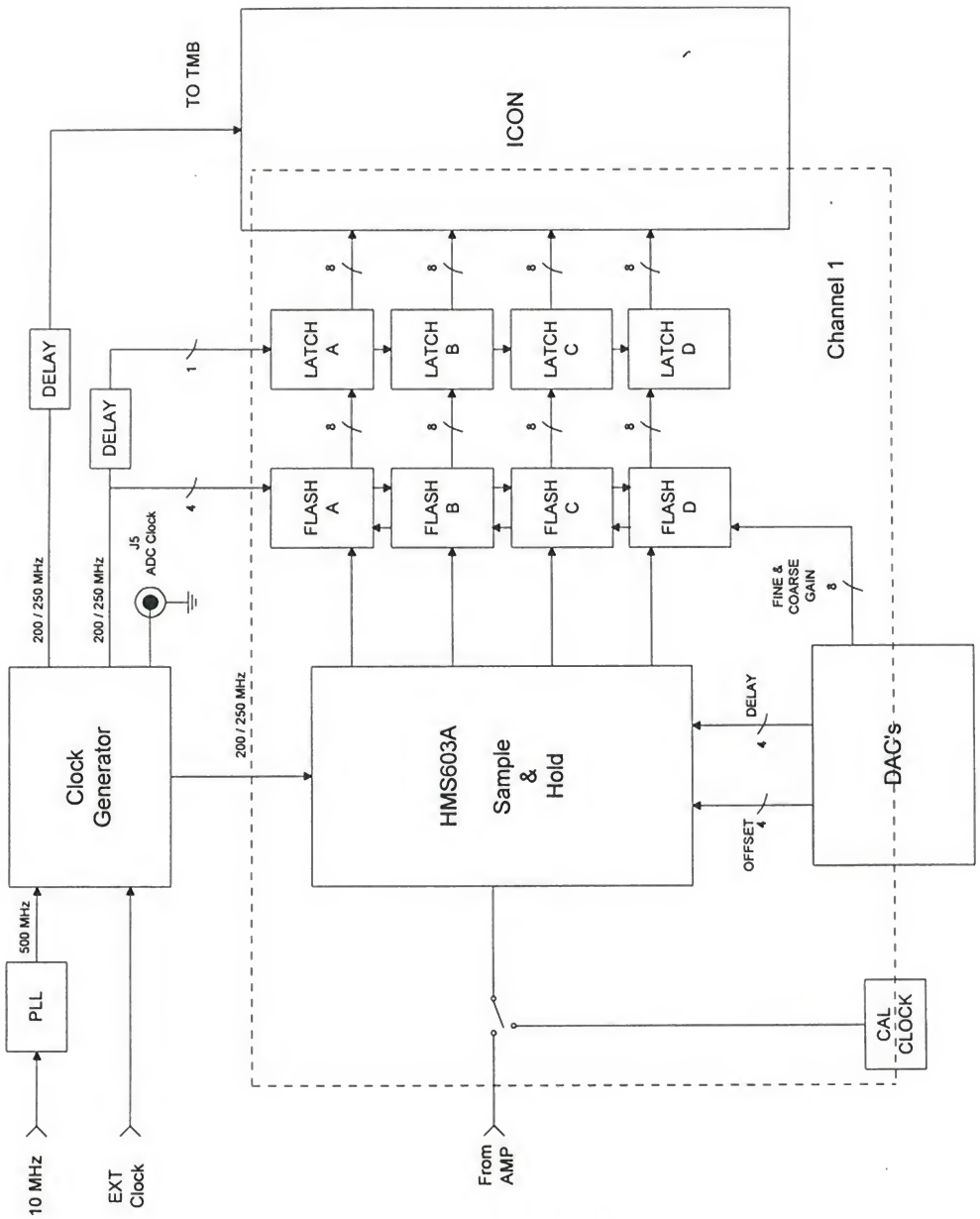

TO TMB
ICON
Channel 1
DELAY
DELAY
LATCH A
LATCH B
LATCH C
LATCH D
FLASH A
FLASH B
FLASH C
FLASH D
J5
ADC Clock
200 / 250 MHz
200 / 250 MHz
200 / 250 MHz
FINE & COARSE GAIN
Clock Generator
HMS603A Sample & Hold
DELAY
OFFSET
DAC's
500 MHz
PLL
CAL CLOCK
10 MHz
EXT Clock
From AMP

Figure 4.2

4.2.1.1 ICON INTERFACE

The ICON interface provides the interconnection of all but two signals between the 7242ADCA and the rest of the module. Power, address; ECL data, TTL data, strobes, and control signals are all received and transmitted via the ICON interface. The only exceptions are the 10 MHz reference clock and the external sampling clock.

Digitized data is transmitted from the ADC to the memory via 64 ECL data lines. The timing of the data with the addresses generated by the timebase are synchronized by the differential clocks ADCCLK0 / ADCCLK0* and ADCCLK1 / ADCCLK1* which are generated by the 7242ADCA.

The amplifier inputs may be connected or disconnected via the control TTL signal ADC_ZERO which is described in section 4.1.3.

The internal and external sample clock selection is controlled by the TTL signal EXTCLKEN which is described in section 4.1.4.

The calibration clock is enabled or disabled by the TTL signal CALCLKEN* which is described in section 4.1.3.

TTL data for DACs is received from the ICON and is synchronized with the address by means of the strobe STR*. Data is qualified as valid with the write strobe WR*. DACs are discussed in sections 4.1.5 and 4.1.6.

The selection of 3 different sampling modes is controlled by the TTL signals MD0 and MD1 which are described in section 4.1.4.

A status TTL signal (LOCK) is generated by the ADC to indicate PLL phase locking.

4.2.1.2 POWER SUPPLY

Power is supplied to the 7242ADCA via the ICON interface. The following supplies are used by the ADC:

voltage	+5.1	-2.1	+8.7	-8.7	+15.1	-15.2
current (ma)	135	1495	358	498	884	692

In addition, the 7242ADCA uses the 24V supply from the ICON interface to generate a regulated -5.2V supply for itself and the other cards in the module.

4.2.1.3 AMPLIFIER INTERFACE

Analog signals from the 7242B amplifier enter the 7242ADCA via two SMB terminated coaxial cables. These signals should be less than 320 mV pp to produce digital codes in the range -128 to +127. The amplifier inputs may be disconnected via software control by asserting the signal ADC_ZERO. This signal enters the 7242ADCA via the ICON interface, and it drives a double throw relay to switch both channels between the amplifier inputs or ground.

Another signal source is generated on the 7242ADCA which allows the response of the ADC to be characterized independent of the amplifier. This signal is a 15.5642 MHz, 160 mV pp square wave with a duty cycle of about 50%. The clock is enabled by the control signal CALCLKEN*.

4.2.1.4 CLOCKS AND PHASE LOCKED LOOP

Operating Modes:

The ADCA can operate at 3 different sampling rates which include 1 Gsa/s, 400Msa/s, and 200Msa/s.

In the 1Gsa/s mode, all 4 flashes are digitizing. They are each clocked at 250 MHz, and are arranged in phase quadrature so that each flash is successively delayed by 1 nsec.

In the 400Msa/s mode, only 2 flashes are digitizing. They are each clocked at 200 MHz, and are arranged with a 2.5 nsec delay between them.

In the 200Msa/s mode, only 1 flash is digitizing, and it is clocked at 200 MHz. The sampling rate is selected via the control signals MD0 and MD1.

MD0 = 0	MD1 = 0	250 MHz 4 flashes
MD0 = 0	MD1 = 1	200 MHz 2 flashes
MD0 = 1	MD1 = 1	200 MHz 1 flash

Clocks:

The clocks are derived from 1 of 2 sources; either an external sample clock or a VCO located on the 7242ADCA. The phase locked loop regulates the frequency of the VCO by dividing it down to 10 MHz and comparing it to the 10 MHz reference clock. The VCO control voltage is adjusted to obtain a locked state. When external clocking is enabled, the phase comparator does not adjust the VCO control voltage, and the VCO is turned off.

Selection of internal or external sample clock is controlled by the TTL signal EXTCLKEN which comes from the ICON interface.

The 10 MHz reference is generated in the 7200 or supplied to the 7200 from an external source.

The PLL duty cycle is between 40% and 60% and the jitter is less than 40 ps. There is a trim to allow adjustment to 50%.

The 7242ADCA also supplies a differential ECL clock signal to the timebase board so it can generate proper address and other memory clocks for storing digitized data.

4.2.1.5 TRACK AND HOLD

Each flash has a dedicated track and hold circuit where the signal is tracked and held for conversion. The track and holds also provide a means of "fine-tuning" the delay between the four or two interleaved flashes for sampling at the 1Gsa/s and 400Msa/s rates. Offset shifts due to the track and hold can also be compensated for by means of an adjustable offset.

The offset and delay adjustment for each flash's track and hold is accomplished by programming a series of 3 8-bit DACs. Thus, since there are 3 DACs per flash, and 4 flashes per channel and 2 channels, we have 3 X 4 X 2 = 24 DACs.

Offset is controlled by 2 DACs. One DAC is a coarse control which has about 16 times the gain of the other offset control DAC. The offset response with respect to the DAC code is linear. The DAC code is a unipolar value in the range 0..255.

Delay of each track and hold is adjustable over the range -200 ps to +200 ps. The delay response is linear with respect to the DAC code.

4.2.1.6 FLASH CONVERTERS

As mentioned above, the 7242ADCA uses 8-bit ADC flash converters. The output of the flashes is inverted since the amplifiers invert signals supplied to the front panel BNC connectors before they are transmitted to the ADC.

The gain of each flash is adjustable by the use of DACs. Each flash has a dedicated 8-bit gain control DAC. The attenuation response with respect to the DAC value is linear.

4.2.1.7 MEMORY INTERFACE

Digitized data is presented as ECL logic levels to the ICON interface for memory storage.

4.2.2 7242 ICON SUBASSEMBLY

The 7242ICON is a back-plane connector board. It provides the connection path for the TTL BUS, the 32 bit ADC Data, and power routing in figure 4.1. The 7242ICON connects the 7242ADCA, 7242BMEM, 7234INTF, and 7234TMB together. It also distributes the supply voltages which are generated on the various module boards. Mounted on the rear of the 7242ICON are a temperature sensor and a thermal switch. The switch will open when the exhaust air at the rear of the module reaches [70] +/- 5 deg. C and interrupt the main module supply.

Each of the four positions on the 7242ICON consist of three 96-pin connectors used for signal and ground connections and one 32-pin connector for supply voltages. Refer to the 7242ICON schematic for pin assignments.

4.2.2.1 SUPPLY VOLTAGES

The 7200 delivers 24V and 24V return along with a clean ground through high current contacts on the rear connector of the 7242B module. The MEM board, which receives this supply, passes the 24V return and ground directly on to the 7242ICON power connectors. The 24V is passed to the 7242ICON where it first travels through the thermal switch before connecting to the power connectors. The various supplies needed in the module are distributed among the MEM, TMB and ADC. The voltages generated on the boards are fed to the power connectors for use by the other boards.

The two center layers of the ICON are ground planes. Connections to these planes are through the center row of pins on each of the 96 pin connectors. This provides a low impedance ground path to all of the module boards. The planes

are also a reference for the ECL transmission lines on the component side of ICON.

4.2.2.2 TTL ADDRESS A0 - A31

The 7242ICON address space is divided into two areas, one for control registers and one for acquisition memory. During data acquisition the TMB has control over the address bus. For a normal acquisition the TMB drives A31-A4. In the case of rollmode, A3 and A2 are driven by the INTF for selecting a long word in memory (internal data storage on the MEM is four long words wide). Since all accesses are on long word boundaries, A0 and A1 are always driven low. The 7234INTF has control of the address bus whenever acquisition is halted.

4.2.2.3 TTL DATA D0 - D63

These 64 lines are used for transferring data between the INTF and TMB for module control and for reading sample data from the MEM. In the case of register access the use of the bits depend on the register function. The bits may be used individually or in groups of various lengths to form control words. When transferring sample data the 32 bit long word represents four 8 bit data samples. Detailed information concerning the data formats can be found in the individual sections for the ADC and MEM.

4.2.2.4 STR0* and WR*

All TTL data accesses within the module require a strobe signal. This is provided by the INTF and labeled STR0*. Also necessary is the signal WR* which controls the direction of data transfer. STR0* is an active low signal which must have a width of at least 150 ns in order to be recognized by the responding circuits.

A read operation occurs when STR0* is true and WR* is false (high).Address and WR* must be valid and stable for the duration of the strobe. Data must be valid 125 ns after the STR0* goes low and must remain until after the strobe goes high. When STR0* goes high the data must be removed within 100 Ns. With WR* true and STR0* true a write operation occurs. During a write cycle, the data, address, and WR* must be valid at least 50 Ns before the leading edge of the strobe and remain stable for 50 Ns after the trailing edge of the strobe.

4.2.2.5 MEMORY CONTROL SIGNALS

MD0 MD1	These two TTL signals originate on the TMB and control the byte stacking mode used by the MDX802 on the MEM and enables one, two, or four flashes on the ADC.
CPE	This TTL signal selects between computer access (by INTF) and acquisition (by ADC). Generated on the TMB.

4.2.2.6 ECL data

These 32 lines provide a high speed path for the digitized data from the ADC. This bus may carry 1, 2, or 4 bytes depending on the number of channels being used.

4.2.2.7 ACQUISITION MEMORY CLOCKS

HCK HCK* VCK VCK* PCK PCK*	These three ECL complimentary pairs of clocks control the byte stacking operation sequence on the MEM. Generated on the TMB.
STOP STOP*	This ECL pair stops/enables the data acquisition on the MEM and originates on the TMB.

4.2.2.8 TIMEBASE CLOCKS AND CONTROL SIGNALS

CALTRG*	ECL trigger signal, synchronized with the calibrate signal. Sent from the ADC to the TMB.
INT*	TTL interrupt from TMB to INTF. Signifies acquisition complete.
MARM*	TTL signal sent by the INTF to arm the TMB. Minimum width - 200 ns
RESET*	TTL module reset generated by INTF. Minimum width - 200 ns
ABORT*	TTL signal sent by the INTF to the TMB to abort an acquisition. Minimum width - 200 ns
CTRIG*	Computer generated TTL trigger sent by the INTF to the TMB. Minimum width - 200 ns
LINE	TTL trigger signal representing the power line frequency. Sent by the INTF.
ADC_ZERO	TTL signal generated on the TMB and used by the ADC to

	switch a zero volt reference into the ADC inputs.
ADCCLK0	ECL sample clock, generated on the ADC and used by the
ADCCLK0*	TMB. Must be 250 MHz, 50% duty cycle +/- 100 ps @ 250 MHz.
ADCCLK1	not used ADCCLK1*
EXTCLKEN	TTL signal, generated on the TMB, enables the external sample clock on the ADC.
CALCLKEN*	TTL signal, generated on the TMB, enables the calibrate signal as an input on the ADC.

4.2.2.9 STATUS SIGNALS

LOCK	TTL signal, generated on the ADC and read by the INTF to indicate that the PLL is locked.
OVLD1*	These signals are true when an overload condition is
OVLD2*	present on the input amplifiers. Generated on TMB and read by INTF.

4.2.3 7242B FRONT PANEL SUBASSEMBLY

The 7242B front panel assembly provides the user interface for the 7242B. Information is input via knobs and buttons. Status is displayed via LED's.

The buttons and LED's all work at standard TTL levels.

The knobs are essentially a series of voltage dividers between +5V and ground. The output of the divider is essentially a DC level between 0 and 5V.

There are two (2) connectors which provide mechanical and electrical connection between the 7234INTF and the 7424B Front Panel. The first connector is a 30-pin AMP part, number 104069-5. The LeCroy part number is 454510030.

1. Var. Gain Pot A	2. Vert. AC Coupling LED
3. Var. Gain Pot B	4. Vert. DC Coupling LED
5. Variable Gain LED	6. Vert. GND Coupling LED
7. Vert./Div Switch	8. Vert. 50 Ohm Coupling LED
9. Var Gain Reset Button	10. Zero Offset LED
11. CH1 Select Button	12. Zero Offset
13. CH1 Select LED	14. Unused CH3 Select Button
15. CH1 50 Ohm LED	16. Unused CH3 Select LED
17. CH1 Overload LED	18. Unused CH3 50 Ohm LED
19. CH2 Select Button	20. Unused CH3 Overload LED
21. CH2 Select LED	22. Unused CH4 Select Button
23. CH2 50 Ohm LED	24. Unused CH4 Select LED
25. CH2 Overload LED	26. Unused CH4 50 Ohm LED
27. No Connection	28. Unused CH4 Overload LED
29. No Connection	30. VCC

The second connector is an 80-pin AMP part, number 104069-3. The LeCroy part number is 454510080.

1. +15V	2. GND
3. Time / Div Switch	4. Time Base Slave LED
5. Trigger Slave LED	6. Interleaved Sampling LED
7. CH1 Trigger Source LED	8. Interleaved Sampling Button
9. Trig Source (Up) Button	10. Display Button
11. Negative Slope LED	12. Ready LED
13. CH2 Trigger Source LED	14. Triggered LED
15. Positive Slope Trig LED	16. AC Trig Coupling LED
17. Ext Trig Source/CH3 LED	18. Trig Coupling (Up) Button
19. Ext/10 Trig Source/CH4 LED	20. LF Trigger Coupling LED
21. Trig Source (Down) Button	22. HF Trigger Coupling LED
23. Trigger Slope Button	24. DC Trigger Coupling LED
25. Line Trigger Source LED	26. Trig Coupling (Down) Button
27. Zero Offset Level LED	28. Zero Delay LED
29. Trigger Level Pot A	30. Trigger Delay Pot A
31. Trigger Level Pot B	32. Trigger Delay Pot B
33. Zero Trig Level Button	34. Zero Trig Delay Button
35. Complex Trigger LED	36. Vertical Coupling (Up) Button
37. Complex Trigger Button	38. Vertical Coupling (Down) Button
39. Vert Offset Pot A	40. Vertical Offset Pot B

Pins 41 to 80 are not electrically connected.

The knobs, buttons, and LED's are arranged in functional sections as indicated below:

Timebase Section:

Timebase Knob	- Selects time per division
Interleaved Sampling Button	- Toggles RIS on/off
Interleaved Sampling LED	- Lit when in RIS

Status Section:

Display Button	- displays most plug-in settings

Trigger Section:

Level Knob	- adjusts trigger threshold level
Delay Knob	- adjusts trigger delay
Source Up/Down Buttons	- allow selection of trigger source
Slope button	- toggles trigger slope
Coupling Up/Down Button	- allow selection of trigger coupling

Trigger Section: (con't)

Level Zero Button	- toggles trigger threshold level between 0V and the previous non-zero level.
Delay Zero Button	- toggles trigger delay between 0 sec and the previous non-zero delay.
Smart Trigger Button	- enables/disables smart trigger
Slave LED	- lit when module is a slave in locked trig operation
Ready LED	- lit when module is armed and acquiring data
Trig'd LED	- lit when module is not-armed
CH1,CH2,LINE,EXT,EXT/10 LED's	- appropriate LED is lit based upon trigger source
POS,NEG LED's	- indicate current trigger slope
AC,LF REJ,HF REJ, DC LED's	- appropriate LED is lit based upon trigger coupling
Zero Delay LED	- lit when trigger delay is 0s
Zero Level LED	- lit when trigger threshold level is 0V
Smart Trigger LED	- lit when in Smart Trigger Mode

Vertical Section:

Fixed Volts per Div Knob	- adjusts v/div on a 1,2,5 sequence

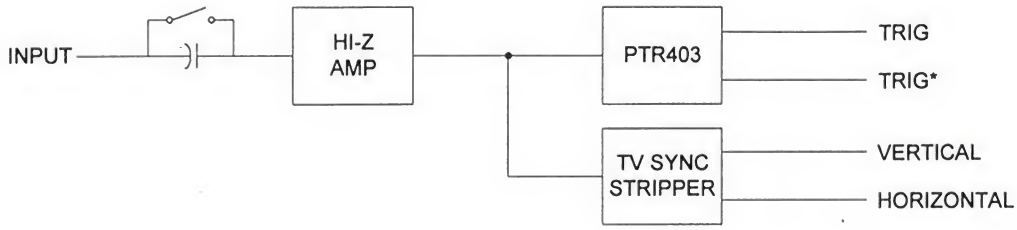
Variable Volts per Div Knob	- adjusts v/div between fixed steps
Offset Knob	- adjusts vertical offset
Var Button	- Toggles variable attenuation between the last knob setting and 1.0
Zero Offset Button	- toggles vertical offset between 0V and the previous non-zero level.
Select Channel Buttons	- selects channel for all coupling, volts per division, variable volts per division, and offset changes.
Variable Volts per Div LED	- lit when v/div is not on a 1,2,5 boundary.
Zero Offset LED	- lit when offset is 0V
AC,DC,GND,DC LED's	- appropriate LED is lit based upon vertical coupling mode.
CH1,CH2 LED's	- lit when channel is selected for parameter change
50 Ohm LED's	- lit when a channel is 50 Ohm DC or GND coupled
OVLD LED's	- lit when input power to CH1 or CH2 BNC exceeds limit while 50 OHM DC coupled.

4.2.4 7242 EXTERNAL TRIGGER SUBASSEMBLY

The external trigger has three major component interfaces which include the signal input, the timebase control/power interface and the differential trigger outputs. See figure 4.3.

The signal input is a single standard BNC connector terminated in 1M Ohms, with a maximum input voltage of 250 VDC. The outputs of the external trigger assembly are the differential trigger outputs as well as Horizontal and Vertical sync pulses if the input signal is a video signal.

The control/power interface to the 7234TMB is accomplished via a 34-pin connector and ribbon cable which is detailed below:



7242EXTR

Figure 4.3

1. GND	2. GND
3. GND	4. VTHET
5. NC	6. NC
7. NC	8. +12V
9. +6V	10. -6V
11. -12V	12. VCC
13. VEE	14. +15V
15. -15V	16. NC
17. TV1	18. TV2
19. NC	20. RACET
21. DIVTET	22. HFREJET*
23. LFREJET*	24. SPET*
25. PTET	26. DCET*
27. BWLET*	28. MA
29. MB	30. Synch Rate1*
31. Synch Rate2*	32. NC
33. NC	34. NC

VTHET - A DC level in the range +/- 8 VDC corresponding to the trigger threshold level. This level must be inverted when HFREJ coupling is selected.

TV1,TV2 - TTL level signals which toggle synchronized to a video synch signal.

RACET - A DC level either at 0 or +12V. When at 0, the external trigger input is DC coupled. When at 12V, the external trigger input is put in series with an RC network for AC coupling.

DIVTET - A TTL level signal indicating that the operator has divided the trigger input level by 10.

HFREJET* - A TTL level signal used to low-pass filter the trigger input up to 50 kHz. No filtering is done when this signal is high. This signal is low only in LFREJ and HFREJ coupling modes.

LFREJET* - A TTL level signal used to reject frequencies below 50 kHz. No filtering is done when this signal is high. This signal is low only in AC coupling.

SPET* - A pair of TTL level signal used to control slope, and
PTET HFSYNCH (divide input frequency by 2).

When both are high, HFSYNCH is enabled.
When SPET* is low and PTET is high NEG slope is selected.
When SPET* is high and PTET is low POS slope is selected.
The slope rules are inverted for HFREJ coupling.

BWLET* - A TTL level signal used to low-pass filter the input signal up to 95 MHz when bandwidth limit is selected. No filtering is done when this signal is high.

DCET* - A TTL level which complements BWLET* except with HFREJ coupling where they are both high.

MA,MB - A 2-bit, 3 combination code for selecting ODD, EVEN, or BOTH TV frames. (TTL levels)

Synch Rate* - TTL levels which form a 2-bit 3 combination code to select a frequency range for TV triggering.

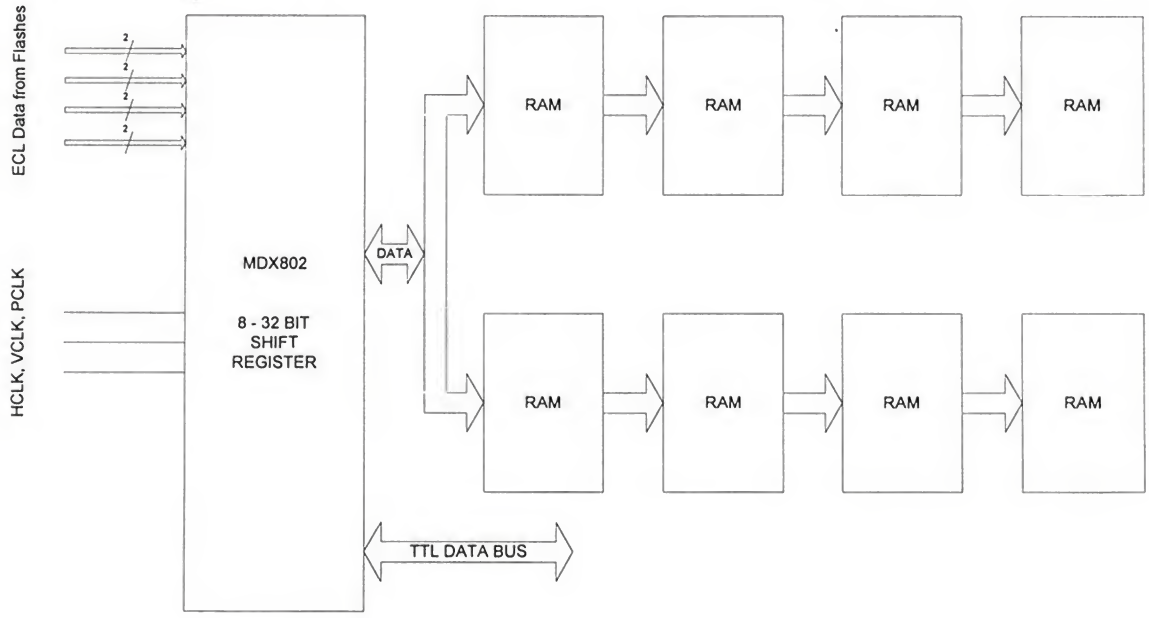
The triggered state differential signal pair is output via two female SMB connector terminated coaxial cables which also connect to the 7234TMB.

4.2.5 7242BMEM

The 7242BMEM board contains the ACQUISITION MEMORY block of figure 4.1, the +5.0 V and -2.0 V DC to DC converters in the POWER block, and part of the INTERFACE to the 7200 mainframe. The 7242BMEM plugs into the 7242ICON. The interface to the 7242ICON is described in section 4.2.4.
The functions of the two blocks of the 7242BMEM board are:

ACQUISITION MEMORY

The ACQUISITION MEMORY is a 256 K byte (1 M with option L1) memory with variable organization. The memory has two I/O ports, one high speed ECL input only port, the second a TTL input/output port. (See figure 4.4)



MEM

Figure 4.4

The ECL input can be configured in one of three ways. First as 32 bit words by 64 K words deep. Second as 16 bit words by 128 K words deep. Third as 8 bit words by 256 K words deep. The 32 bit ECL input is divided into four bytes as shown in the following table.

ECL	number of flashes		
data word bits	four	two	one
0 - 7	flash D	-	-
8 - 15	flash C	flash C	-
16 - 23	flash B	-	-
24 - 31	flash A	flash A	flash A

The TTL port is configured as 32 bit words by 64 K words deep. The 32 bit TTL output word is divided into four data bytes as shown in the following table.

TTL output	number of flashes

data word bits	four	two	one
0 - 7	flash D	1'st flash C	1'st flash A
8 - 15	flash C	1'st flash A	2'nd flash A
16 - 23	flash B	2'nd flash C	3'rd flash A
24 - 31	flash A	2'nd flash A	4'th flash A

The 32 bit TTL input word also contains four data bytes as shown in the following table.

TTL input data word bits	number of flashes four	two	one
0 - 7	flash D	1'st flash C	1'st flash A
8 - 15	flash C	1'st flash A	2'nd flash A
16 - 23	flash B	2'nd flash C	3'rd flash A
24 - 31	flash A	2'nd flash A	4'th flash A

The 7242MEM is divided in such a way that each block of memory (as shown in Figure 4.3) has as its input data from 2 bits from each flash. In this way all of memory can be addressed when only one flash is being used (5 ns/pt or slower). This distribution is shown in the diagram of the board layout shown in figure 4.5.

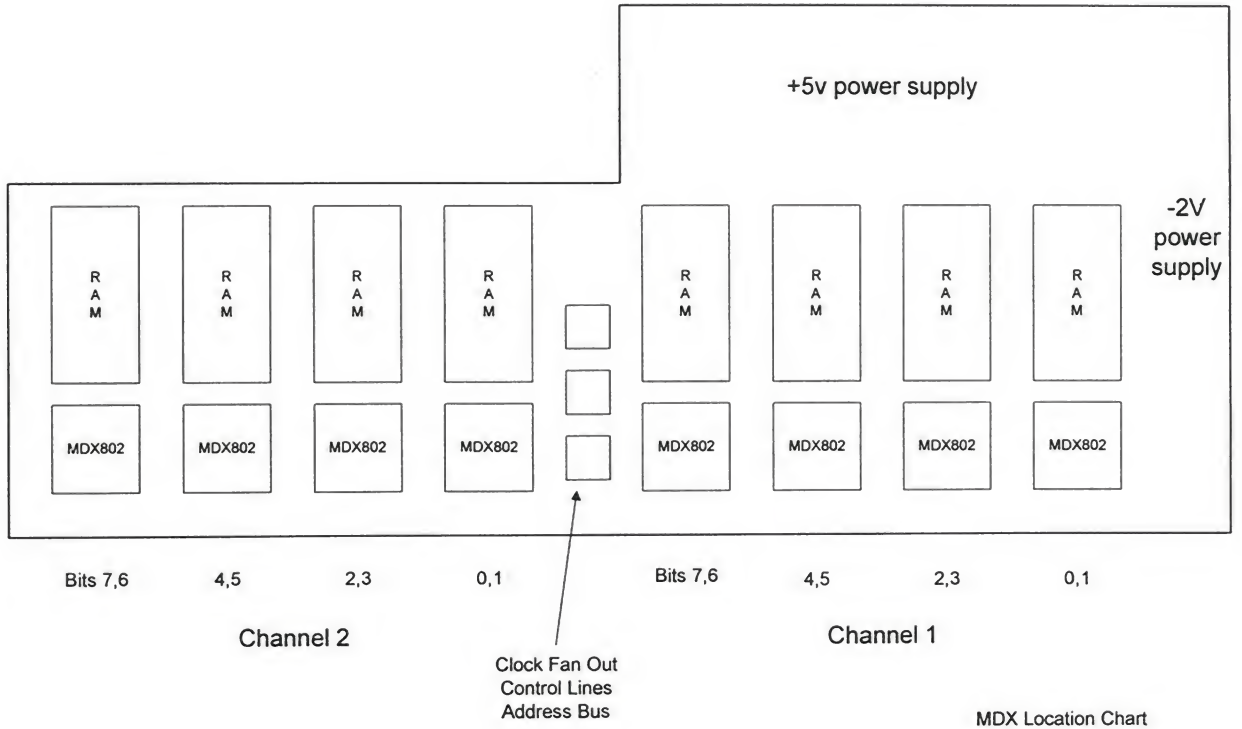


Figure 4.5

7242BMEM(A)

MDX Location Chart

Flyer Size	BIT	CH1	CH2
4 Major Divisions	7	U3	U70
2 Major Divisions	6	U3	U70
1 Major Division	5	U17	U85
1/2 Major Division	4	U17	U85
1/4 Major Division	3	U31	U99
1/8 Major Division	2	U31	U99
1/16 Major Division	1	U45	U113
1/32 Major Division	0	U45	U113

INTERFACE

The 7242BMEM holds the hybrid connector which connects to the 7200 mainframe. This connector contains seven special contacts. Their type and function are described below.

Name	Type	Function
24 V	power	module power
24 V rtn	power	module power
GND	power	module ground
EXT CLK	co-ax	external sample clock
REF CLK	co-ax	10 MHz reference
TRIG IN	co-ax	trigger bus input
TRIG OUT	co-ax	trigger bus output

POWER The 7242BMEM provides -2.0 V and +5.0 V power for the module via the 7234ICON.

4.2.6 7234TMB

The 7234TMB board contains the TIMEBASE and TRIGGER blocks of figure 4.1 It also contains the +15,-15,+8.5 and -8.5v DC to DC converter in the power block and control circuits for CH1 and CH2 amplifiers in the AMPLIFIERS block. The 7234TMB plugs into the 7242ICON and connects to the 7242AMP via two 34 conductor cables and the 7242EXTR via one 34 conductor cable. The interface to the 7242ICON is described in section 4.2.4. The interface to 7242AMP is described in section 4.3.1. (See figure 4.6)

Timebase
The timebase functions include sample rate generation, memory clock and address generation, trigger delay, trigger time measurement (TDC), time stamp generation, and pretrigger delay. The memory clocks can select between 1, 2, or 4 flash mode for the 7242 and between 1, 2, or 4 channel mode for the 7234.

Trigger
The trigger functions include trigger selection, event counting, trigger gating, and trigger latching. For the 7242 the 7234TMB may select vertical and horizontal TV sync inputs from the external trigger input.

Amplifier Controls
The 7234TMB also contains the control registers for control and calibration of channels one and two. For the 7242 the 7234TMB contains control registers for control of the external trigger input.

+/- 15 Volt and +/- 8.5 Volt Generation from +24 Volts

The DC to DC converter on the 7234TMB produces the following output voltages.

+15.0 V.	at	1.5 A.
-15.0 V.	at	1.0 A.
+8.5 V.	at	0.5 A.
-8.5 V.	at	0.5 A.

The 7234TMB controls three major functions during data acquisition in the 7234 plug-in, sample rate, writing to memory, and trigger. The 7234TMB also controls the Channel 1, Channel 2, and External front end modules. The 7234TMB schematic breaks these functions into the following blocks :

Sample rate generator
Memory clocks generator
Memory address generator
Time stamp generator and pretrigger delay
Time to digital converter (TDC)
Trigger delay
Trigger selection
Event counter
Trigger gate
Trigger latch
Front end control
DC to DC converter

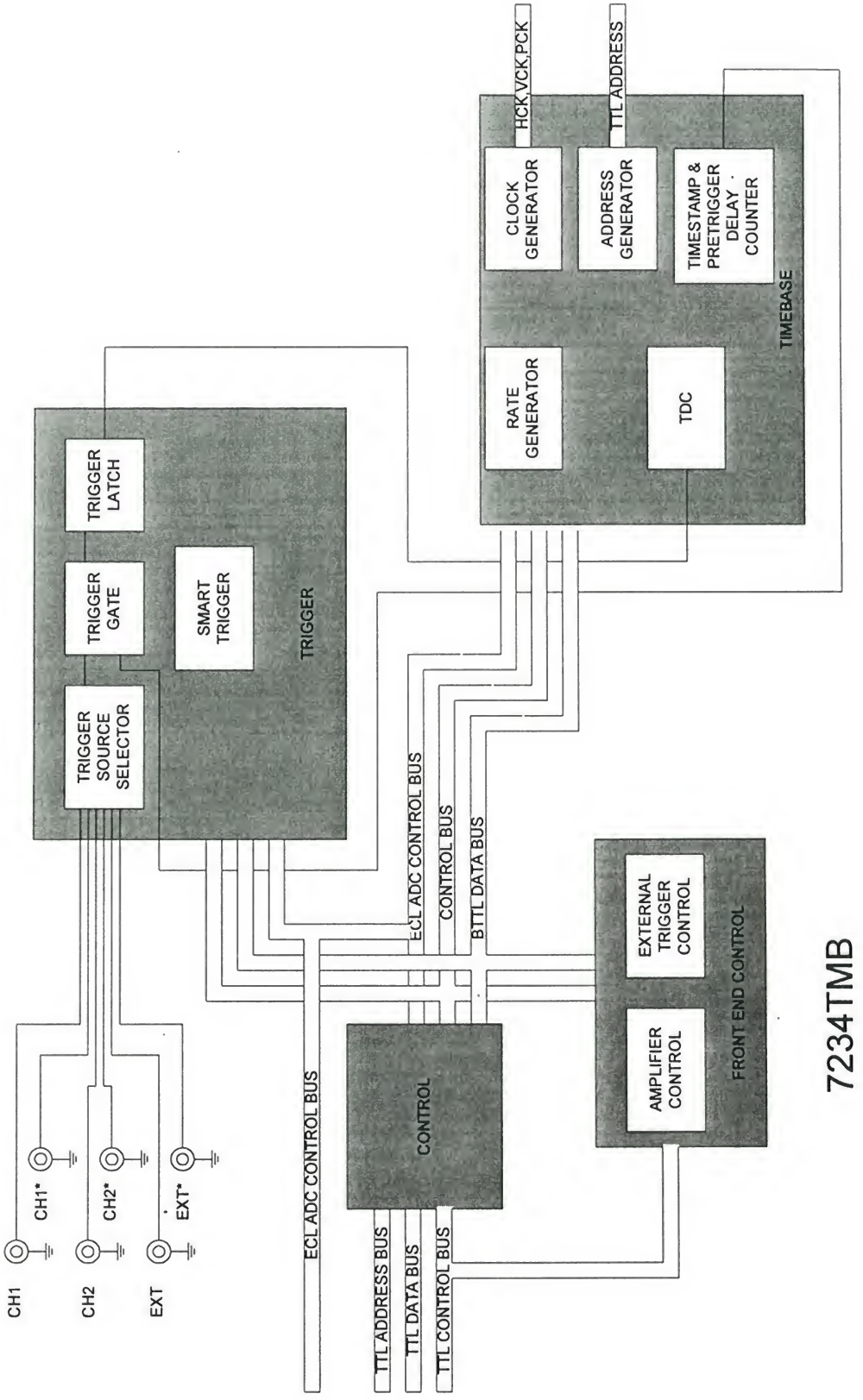

HCK,VCK,PCK
TTL ADDRESS
CLOCK GENERATOR
ADDRESS GENERATOR
TIMESTAMP & PRETRIGGER DELAY COUNTER
TIMEBASE
RATE GENERATOR
TDC
TRIGGER LATCH
TRIGGER GATE
SMART TRIGGER
TRIGGER
TRIGGER SOURCE SELECTOR
ECL ADC CONTROL BUS
CONTROL BUS
BTTL DATA BUS
EXTERNAL TRIGGER CONTROL
AMPLIFIER CONTROL
FRONT END CONTROL
CONTROL
CH1*
CH2*
EXT*
CH1
CH2
EXT
ECL ADC CONTROL BUS
TTL ADDRESS BUS
TTL DATA BUS
TTL CONTROL BUS
7234TMB

Figure 4.6

The sample rate generator adjusts the sample rate by dividing the ADC clock to produce the memory clocks. Lower sampling rates are produced by dropping data samples before being clocked into the memory. Three memory clocks are generated allowing data to be collected from four, two, or one of the flash ADC's. This allows the acquisition memory to be shared by one, two, or four channels in the 7234 and the interleaving of up to four flashes in the 7242. The 22 bit sample address is generated for the memory card. The 64-bit time stamp counter records the timing between segments in sequence mode. The trigger once enabled by the pretrigger delay counter is latched and fed to the TDC. The TDC measures the time between the trigger and the 64 sample clock making random interleaved sampling (RIS) possible. Pretrigger delay insures that all of the samples in the data record are valid. Once the TDC synchronizes the trigger to the 64 sample clock, the trigger delay counter counts down in 64 sample blocks and then stops the acquisition.

The trigger selector selects from the various trigger sources to produce two triggers, Trig_A and Trig_B. Trig_A via the trigger gate and latch triggers the acquisition stop. Trig_A can also clock the event counter. Trig_B restarts the event counter and enables the trigger gate. For simple triggers Trig_B is disabled and the trigger gate is enabled. For smart triggers Trig_B and the event counter are used to control the trigger gate enable. Thus allowing the following smart trigger modes:

Holdoff
State qualified
Time qualified
TV trigger

The front end control produces several digital and analog signals which control the channel 1, channel 2, and external front end modules via three 34 pin connectors. The external control is only used in the 7242. The digital signals are driven by several registers. The analog signals are produced by a small memory and scanner. The scanner takes data from the memory and drives a DAC. The output of the DAC drives several sample and hold circuits to adjust analog controls in the front end modules.

4.2.6.1 TIMEBASE

Schematic sheets 4 through 11 describe the timebase for the 7234TMB. Sheet 4 is a top level schematic of the timebase with the trigger delay counter. Sheet 5 contains the sample rate generator. Sheets 6 and 7 contain the memory clock and address generator. Sheet 8 contains the time stamp and pretrigger holdoff counters. Sheets 9, 10, and 11 contain the TDC. The timebase has two main inputs, the clock from the ADC and the latched trigger from the trigger section.

For the 7242 the clock input is either 250 MHz or 200 MHz. In the 7234 the clock is always 200 MHz. The main outputs of the timebase are the memory clocks and addresses.

Sheets 9, 10, and 11 contain the TDC circuit. Both the ADC clock and the trigger inputs go to the TDC. On sheet 9 these signals are the inputs to the HTD405. The ADC clock is buffered and distributed to the sample rate generator and the coarse and fine counters of the TDC. The TDC measures the time between the trigger and the synchronized trigger. The TDC synchronizes the trigger input to add<5>, 64 sample boundaries. In the 7234 these 64 samples are divided among the enabled channels. The TDC output, synchronous trigger, starts the trigger delay counter. The TDC measures the time before the 64 sample boundary in two parts. A fine measurement determines the time between the trigger and the next ADC clock. A coarse measurement counts the ADC clocks between the trigger and the 64 sample boundary. 16 and 40 bit registers hold the fine and coarse counts respectively. Sheet 10 contains the coarse counter. Sheet 11 contains the fine counter.

The TDC makes the fine measurement by expanding the time between the trigger and the second ADC clock by a factor of 1000. The expanded interval is measured by counting the ADC clock with the counter on sheet 11. The expansion produces a resolution of about 4 ps for a 250 MHz clock and about 5 ps for a 200 MHz clock. The fine measurement can take up to 12 us to complete, therefore the output TDC_BUSY* holds-off the data ready interrupt until the conversion is complete. If needed, the fine measurement and its hold-off can be disabled. The fine and coarse registers require another 500 ns to settle after the interrupt is released. The fine measurement has significant temperature and unit to unit drifts and therefore requires a periodic calibration for gain and offset. The HTD405 provides the means for this calibration by using the CTRIG* input from the ICON bus to generate a trigger synchronous with the ADC clock. The HTD405 then controls the delay between the clock and this trigger with an analog input. A 16 bit control word sets this delay with about 0.2 ps per lsb resolution.

The sample rate generator, schematic sheet 5, accepts the buffered ADC clock from the TDC. Two counters are used to divide the ADC clock. The divided down clock produces the memory clocks. In this way, the ADC's sample rate is reduced by dropping samples as they are clocked into the acquisition memory. The counters can divide at a maximum rate of 200 MHz. In both the 7242 and 7234 the sample rate generator operates the same way. For 1Gsamples per second, the highest sampling rate, the 250 MHz clock is passed straight through. For all other sampling rates, 400M to 0.01 samples per second, the ADC clock is 200 MHz. Two counters divide the 200 MHz clock producing sample rates from 100 M to 0.01 samples per second. The sample rate generator is controlled by three registers, one 8 bit and two 16 bit. For the 8 bit register the 4 lsb's, bits 0 -

3, set the dividing rate of the high speed divider. Bits 4 and 5 control the memory clock generator. Bits 6 and 7 are spare. The 16 bit registers form a 32 bit control word for the low speed divider.

Sheet 6 contains the memory clock generator and sheet 7 the memory address generator. The 7234TMB can use either the 7234MEM or the 7242BMEM as acquisition memory. The 7234TMB generates three memory clocks which control the demultiplexing of data samples into the acquisition memory. Adjusting the relative period of these clocks selects data from four, two, or one of the channels on the 7234ADC and four, two, or one of the ADC's in each channel on the 7242ADCA. The sample clock also generates a 22 bit sample address for the 7242BMEM board as shown on schematic sheet 7. Since the memory board stacks data into 16 sample words, 128 bits, only A <4:21> are generated by the timebase, A <0:3> are not driven. The addresses A <4:21> change at maximum rate of 62 MHz. The MCT402 counts at a maximum of 25 MHz. Therefore the master clock, MCLK, which drives the address counter as well as all the other timebase functions must run at maximum rate of 15 MHz and counts 64 sample boundaries. In the 7234 these 64 samples are divided among the enabled channels. With one channel enabled MCLK counts 64 sample boundaries. With two channels enabled it counts 32 sample boundaries for each channel. And with four channels enabled the counters count 16 sample boundaries for each channel. After each trigger, when sampling stops, the 64 sample address is stored to mark the beginning of the data record. This 16 bit word holds the start address, A <6:21>, in bits 0 - 15. The address counter also contains a 16 bit segment size counter. When the segment size counter times out the address counter is reloaded with the segment start address making the acquisition memory circular. The 16 bit counter allows segment sizes from 64 samples to 64 K samples. Again the segment size is divided by the number of enabled channels in the 7234. When multiple segments are recorded, each segment's start address must be loaded into the address counter by the 7242INTF card between segment acquisitions.

Schematic sheet 8 contains the time stamp and pretrigger holdoff counters. These counters are implemented using MCT402's. The time stamp counter measures the time between segment triggers. This 64 bit counter runs continuously counting in 64 sample increments while the sample rate is unchanged. Again for the 7234 the 64 sample increments are divided by the number of enabled channels. The counter is reset by the system reset and at the fastest sampling rate will take over 37 thousand years to overflow. The counter output is latched when a trigger occurs and is held in four 16 bit registers.

The pretrigger delay counter disables the trigger latch until the pretrigger samples have been written. This 32 bit counter counts in 64 sample increments and latches its output when the trigger occurs. Remember, the 64 sample

increments are divided by the number of enabled channels in the 7234. When the pretrigger delay is disabled, this latched output allows the valid portion of the data record to be determined. The counter is read and written as two 16 bit registers.

Sheet 4 contains the trigger delay counter. An MCT402 is used as the 32 bit delay counter. The synchronized trigger starts the counter which stops the acquisition after counting down the delay. This 32 bit counter counts in increments of 64 samples and is controlled by two 16 bit registers. As before, in the 7234 the 64 samples are divided among the enabled channels.

4.2.6.2 TRIGGER

Schematic sheets 12 through 19 describe the trigger circuit of the 7234TMB. Sheet 12 is a top level schematic of the trigger circuit. Sheet 13 contains the trigger selector. Sheets 14, 15, 16 and 17 contain the event counter. The falling edge delay on sheet 15, load synchronizer on sheet 16, and 36 bit counter on sheet 17 makeup the event counter. Sheet 18 contains the trigger gate. Sheet 19 contains the trigger latch. The trigger circuit has three main inputs. These are the trigger signals from the channel 1, channel 2, and channel 3 for the 7234 or external trigger for the 7242. The main output of the trigger circuit is the latched trigger. The latched trigger is fed to the TDC in the timebase where it initiates the acquisition stop.

Schematic sheet 13 contains the trigger selector. The trigger selector selects from the many trigger inputs to produce the outputs TRIG_A and TRIG_B. TRIG_A and TRIG_B can be produced from the following sources:

TRIG_A		TRIG_B	
7242	**7234**	**7242**	**7234**
CH 1	CH 1	CH 1	CH 1
CH 2	CH 2	CH 2	CH 2
EXT	CH 3	EXT	CH 3
LINE	LINE	TRIG_A_DEL	TRIG_A_DEL
CALTRG	CALTRG	TV1	
TV2			

The differences in the trigger selectors between the 7242 and 7234 are that CH3 replaces EXT and the 7234 does not have TV trigger. The differential inputs CH1, CH2, and CH3 or EXT are received by 10H116's and wire-or'ed to the output of a 10H101 before being fed to the 10H121, "OR AND", which does the selection. The wire-or provides additional isolation between the trigger inputs.

The other selector inputs are single-ended signals. The output of the selector is then passed through 10H107, "XOR", to allow the output polarity to be changed. Selecting more than one source for TRIG_A or TRIG_B forms the logical AND of the sources. Since the polarity of the trigger sources and output of the selector can be changed, one can produce the "AND" or "OR" of any combination of channels 1, 2, and 3 or external. The trigger selector is controlled by a 16 bit register. The four msb's of this register control the trigger gate and trigger latch. Sheet 14 contains the top level schematic of the event counter. The event counter's inputs are TRIG_A, TRIG_B, the trigger gate output, and a 100 MHz clock. Either TRIG_A, TRIG_B, or the trigger gate output are used by the load synchronizer, sheet 16, to start the 36 bit counter, sheet 17. Either TRIG_A or the 100 MHz clock are selected to increment the 36 bit counter, sheet 17. For short delays TRIG_A or TRIG_B can be delayed by 1 ns to 50 ns by the falling edge delay, sheet 15. The outputs of the 36 bit counter and the falling edge delay are combined to drive the enable to the trigger gate. Since the selectable start and count signals are asynchronous, the start is synchronized to the count signal before driving the counter load input. A five bit ECL counter and 32 bit TTL counter form the 36 bit counter. This counter produces time intervals from 10 ns to 500 s and counts up to 50 billion events. The short delay, 1 ns to 50 ns, is produced by a controlled current source to adjust the discharge time of a capacitor. Three 16 bit registers control the operation of the event counter. One selects the start and count signals the other two are the msb's of the 36 bit counter.

The trigger gate, sheet 18, passes the trigger to the trigger latch only when enabled by the event counter. The trigger gate can be armed in two ways. When in automatic mode, the trigger gate rearms once a trigger is passed. When the trigger gate enable is used to rearm the trigger gate, only restarting the event counter will rearm the trigger gate.

The trigger latch, sheet 19, when enabled by the pretrigger delay counter latches the trigger signal passed by the trigger gate. The pretrigger delay insures that all pretrigger samples are acquired before a trigger is latched. Once latched, the TDC synchronizes the trigger for the trigger delay counter.

The trigger bus allows different modules to use the same trigger in a master and slave arrangement. The three msb's of the trigger selector control word control the trigger bus. If both the internal and trigger bus are enabled the logical AND of the two signals is passed as the latched trigger. The trigger bus output is the latched trigger from the master module. Only one module may have its trigger bus output enabled at a time.

The trigger master must be set with the maximum pretrigger delay of all the modules slaved to it and itself. The trigger bus is a 50 ohm coax bus which should be terminated with 50 ohms, although it will operate without the

termination. With 50 ohm termination the trigger levels are 0.0 Volts and -0.8 Volts. Without the termination the active low trigger signal level is -1.6 Volts. The high level remains at 0.0 Volts. The trigger bus is brought to the 7200 rear panel for connection to an external crate.

4.2.6.3 ICON INTERFACE

Sheet 20 contains the ICON interface and control. The Interface circuit consists of data buffers, a control register, and four PAL's. Three of the PALS do address decoding. The fourth does random logic. The PAL programs can be found in appendix A.

4.2.6.4 AMPLIFIER CONTROLS

Schematic sheets 21 through 27 describe the control circuits for the CH 1, CH 2 and EXT amplifiers. Sheets 21 and 22 contain the scanning DAC. Sheet 23 contains the EXT control register and the calibration attenuator. Sheet 24 and 25 contain the control for channel 1. Sheet 26 and 27 contain the control for channel 2.

Sheet 22 contains a 10 MHz R C oscillator made with 74HCT04's which drives a counter to divide this clock by twenty. These clocks drive a sequencer made from 74HC74's and the MCL404. The sequencer provides the proper timing of data and strobes for the MCL404 on sheet 21. The MCL404 contains twelve 16 bit registers which are output to the DAC in sequence. The MCL404 also generates control signals for the sample and holds circuits. The MCL404 requires 16 cycles of the clock CK2U to update one sample and hold circuit. The time to update all 12 sample and hold circuits is 12 X 16 X 20 X the period of the R C oscillator.

Sheet 23 contains the control register for external trigger input. This 16 bit register drives 11 TTL signals and 1 relay via a 2003, open collector transistor buffer. The calibration signal CAL_IN from the sample and hold on sheet 21 drives a selectable, X1, X10, and X100, attenuator. This attenuator increases the dynamic range of the calibration signal. Separate OP-27's and HA5002's buffer the attenuator output for each channel. Also shown on sheet 23 are the power supply filters for the external trigger module.

Sheets 24 and 26 are identical and contain the digital control signals for channels one and two respectively. Each channel's control consists of a 16 bit register which drives 6 FET switches via 1488 RS-232 drivers, 6 relays via 2003 open collector transistor buffers, and 5 TTL signals which are not buffered. The overload output from the amplifier is monitored by an LM339. The LM339 drives

the overload signal on the ICON bus and forces the calibrate input to open the input of the amplifier. All of the signals are filtered to reduce the noise in the amplifiers. Also shown are the power supply filters for each channel.

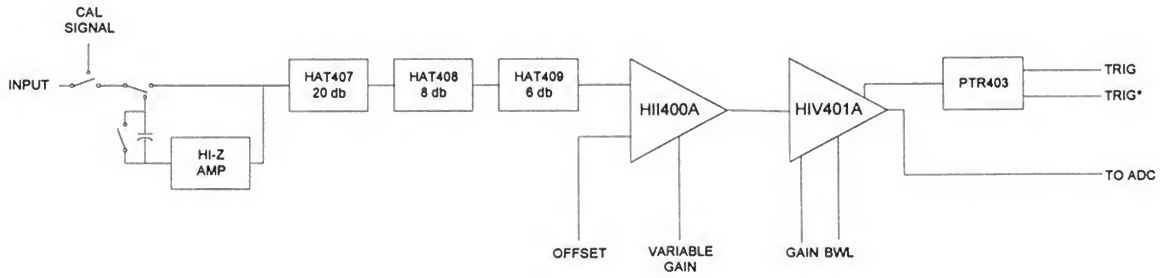
Sheets 25 and 27 contain the analog control signals for both channels. These signals are generated from the output of the scanning DAC with sample and hold circuits using DG201 switches, NPO hold capacitors, and LF353 FET input op-amps. Besides the four control signals, each channel's calibration signal is buffered by separate OP-27's and HA5002's.

4.2.6.5 DC TO DC CONVERTER

Schematic sheet 28 describes the DC to DC converter.

4.2.7 7242AMP

The 7242AMP module contains the signal conditioning amplifiers for CH1 and CH2 in the AMPLIFIERS block. The 7242AMP is connected to the 7234TMB via two 34 conductor cables. The interface to the 7234TMB is described in section 4.3.1. (See figure 4.7)



7242AMP
Figure 4.7

4.3 SUBASSEMBLY INTERFACES

4.3.1 ADC, TMB, AMP INTERFACE

The 7242AMP is controlled via two 34 conductor cables connected to the 7234TMB. Each of the cables controls an input channel with exactly the same signals and pin assignments. The signals and pin assignments are:

Pin	Signal	
1	RCAL	relay to open input and connect cal signal
2	RHZ	relay to enable 1 Mohm input
3	RAC	relay to enable AC coupling
4	RATTA	relay to enable attenuator A
5	RATTB	relay to enable attenuator B
6	RATTC	relay to enable attenuator C
7	HZDIVT	enable 1 Mohm divide by ten
8	HZDIVT*	not enable 1 Mohm divide by ten
9	HFREJ	enable HFREJ trigger coupling
10	LFREJ*	not enable LFREJ trigger coupling
11	GAIN A	enable amplifier gain A
12	GAIN B	enable amplifier gain B
13	BWL	enable input band width limit
14	SP*	not enable trigger prescaler
15	PT*	not enable positive trigger
16	DCTR	enable DC trigger coupling
17	BWLTR	enable trigger band width limit
18	+5 V	+5.0 volts at 100 mA
19	5.2 V	5.2 volts at 425 mA
20	+12 V	+12.0 volts at 550 mA
21	+6 V	+6.0 volts at 125 mA
22	6 V	6.0 volts at 275 mA
23	12 V	12.0 volts at 200 mA
24	OVLD	input overload
25		spare
26	VTH	trigger threshold
27	VARGAIN	variable gain control
28	HZOFF	offset control for 1 Mohm input
29	LZOFF	offset control for 50 ohm input
30	GND	ground
31	GND	ground
32	GND	ground
33	CAL	calibration signal
34	CALSNS	calibration sense

Signals RCAL through RATTC drive 12 volt relays. Each coil is energized by pulling the signal line to ground. The driver must sink at least 20 mA and have an output high voltage of 12 volts. Signals HZDIVT through BWLTR drive FET switches. These signals must swing from -12 to +12 volts supplying minimal current (100 uA). OVLD swings from -5.0 to +5.0 volts supplying up to +/- 10 mA. When OVLD is greater than 0.86 V, an input overload has occurred. Signals VTH through LZOFF are analog control signals with swings of +/- 10 volts and supplying at least +/- 10 mA of current. CAL is an analog control signal capable of driving 50 ohms to +/- 5 V. CALSNS is a remote sense for CAL.

4.3.2 INTF, FRNT INTERFACE

4.3.2.1. INTRODUCTION

The major sections of the 7234INTF are as follows:

A. VME SECTION
- |------- VME INTERFACE
- |------- LOCAL VME RESOURCES
  - |---------- EEPROM
  - |---------- FRONT PANEL I/O
  - |---------- VME STATUS/CONTROL REGISTERS
- |------- GLOBAL BUS INTERFACE
- |------- VME INTERRUPT HANDLER/CONTROLLER

B. TMS PROCESSOR SECTION
- |------- LOCAL RESOURCES
  - |---------- UVPROM
  - |---------- LOCAL MEMORY
  - |---------- STATUS/CONTROL REGISTERS
  - |---------- MIN/MAX GATE ARRAY
  - |---------- PAGE REGISTERS
  - |---------- VME INTERRUPT REQUEST
- |------- GLOBAL BUS INTERFACE

C. GLOBAL BUS SECTION
- |------- BUS ARBITOR
- |------- GLOBAL MEMORY
- |------- ICON INTERFACE

(See figure 4.8)

4.3.2.2. VME SECTION (VME INTERFACE)

The actual interface between the INTF board and the VME back- plane contains the following:

A. ADDRESS BUS BUFFERS
B. DATA BUS BUFFERS
C. VME INTERFACE CONTROLLER

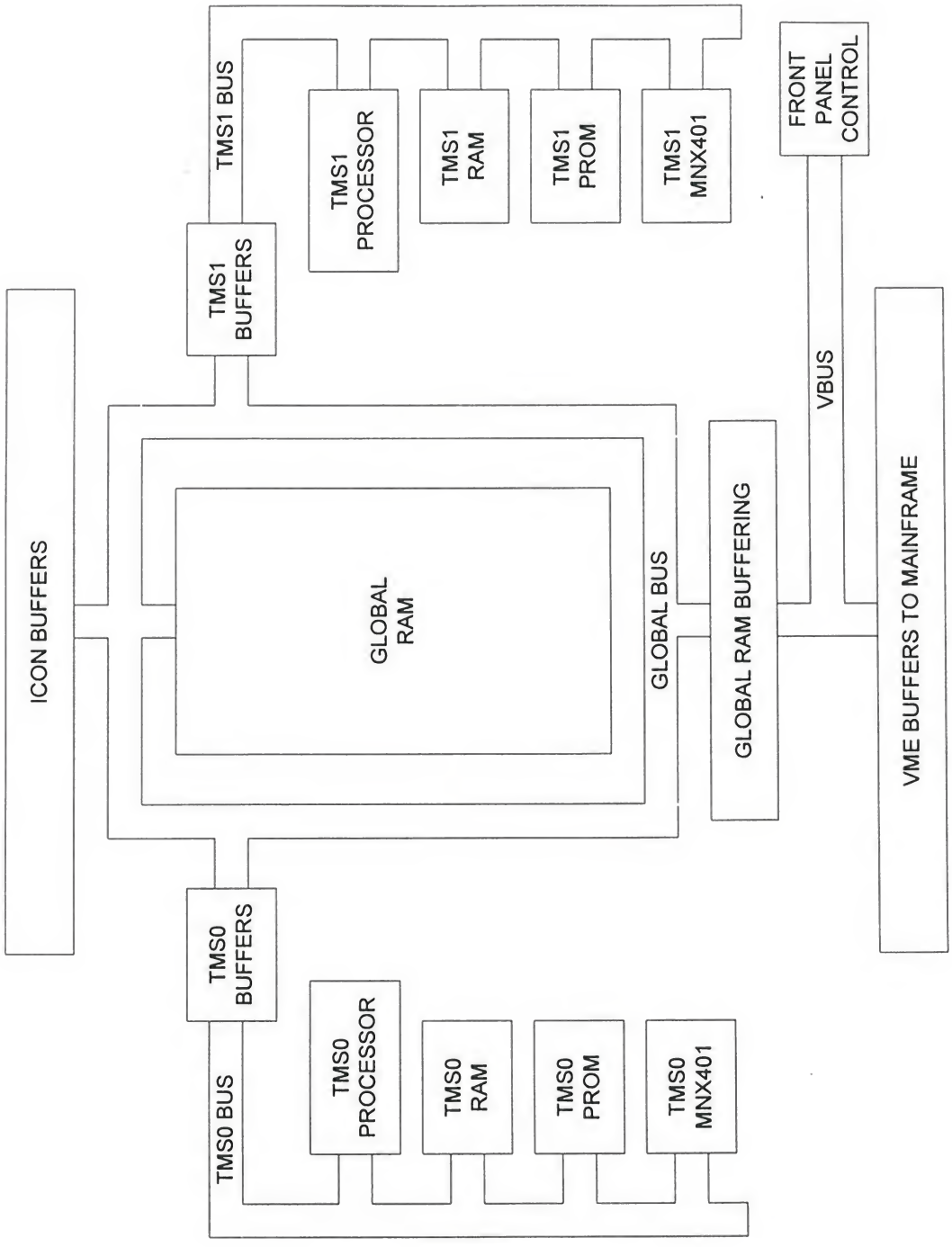

TMS1 BUS
TMS1 PROCESSOR
TMS1 RAM
TMS1 PROM
TMS1 MNX401
FRONT PANEL CONTROL
TMS1 BUFFERS
VBUS
ICON BUFFERS
GLOBAL RAM
GLOBAL BUS
GLOBAL RAM BUFFERING
VME BUFFERS TO MAINFRAME
INTF
TMS0 BUFFERS
TMS0 BUS
TMS0 PROCESSOR
TMS0 RAM
TMS0 PROM
TMS0 MNX401

Figure 4.8

A. ADDRESS BUS BUFFERS

The address bus buffers are simply just as the name implies. They are used to buffer the VME address bus from the backplane to be used as address lines within the INTF board without causing excessive load on the backplane. There are some mechanical and electrical restrictions that must be satisfied in order to comply with the VME bus specification. The address bus buffers are made up of 3 octal non-inverting buffers (type 74als541). Since the INTF board is suppose to be an A24 type of interface (using 24 address lines) and since the VME bus does not have an A0 address line, there remains a spare buffer in the hardware described above. This spare buffer is used to buffer the VME WRITE strobe for the same reasons that the address lines were buffered.

B. DATA BUS BUFFERS

The data bus buffers are again simply just as the name implies with some major differences. First of all since the data bus is bi-directional, the buffers must become transceivers allowing the data bus to operate either as an input to the INTF board or as an output from the INTF board. Since the INTF is suppose to be a D16 type (using 16 data lines for all transfers), we need 2 octal transceivers (type 74als645). These transceivers will be controlled by the VME interface controller described below in terms of when they are enabled and what direction is required for the data bus on any given transfer.

C. VME INTERFACE CONTROLLER

The purpose of the VME controller is to serve as the intelligence for allowing the VME backplane to communicate with the INTF board. The controller consists of a single PAL (programmable array logic) device (type 22v10). The primary function of this controller is to decode when the activity that occurs on the VME backplane requires the INTF board to become involved. The signal that indicates that the present transfer cycle requires the INTF board to become involved is the "N" line of the backplane. When this line becomes asserted the present VME transfer cycle should more than likely involve the INTF board. The decision of whether or not the present VME cycle is appropriate for the INTF board to get involved is based on the status of 8 other lines from the backplane. They are:

1. VME write*
2. address line #20
3. address line #21
4. address line #22
5. data strobe 0*
6. data strobe 1*

7. iack*
8. long word*

Depending on the status of these lines, we are able to determine to what resource of the INTF board the VME backplane wishes to communicate with and if the requested mode of communication is correct for that resource. The possible resources with the correct mode of communications are listed here.

1. EEPROM	word read/write
2. FRONT PANEL	word read/write
3. STATUS/CONTROL REGISTERS	word read/write
4. GLOBAL BUS	word read/write long read only

For all resources except the request for the global bus, the controller simply generates the output signal called "general I/O" and then waits an appropriate amount of time before issuing a "DTACK" back to the backplane indicating that the transfer is complete. When the VME cycle is an access to the global bus, the controller issues the signal called "VME_BUS_REQ" to the bus arbitor and then waits for the arbitor to say that the cycle is complete. At this time the controller decides whether or not the VME request was a long access. If not, the VME hand- shake is completed via "DTACK". If a long access was requested the controller increments the least significant address line (called "GVA1") and again makes a bus request to the arbitor. Now when the arbitor completes this cycle the controller completes the VME handshake via "DTACK" and presents the backplane with 32 bits of data. It should be noted that any invalid VME transfer request made to the INTF board will result in the handshake not being completed via "DTACK". This will result in the VME CPU board timing out and issuing a bus error.

4.3.2.3. VME SECTION (LOCAL VME RESOURCES)

Local VME resources is defined as those resources on the INTF board that are accessible only by the VME backplane as opposed to those resources that are accessible by both the VME backplane and the TMS processors that on the board. The local VME resources include the following:

A. EEPROM
B. FRONT PANEL I/O
C. VME STATUS/CONTROL REGISTERS

The selection for which one of the local resources is desired is done by decoding of the following signals:

1. General I/O from the VME controller described above
2. VME address line #17 through #19 for the address buffers
3. VME write strobe for the address buffers

This decoding is done in two 3 line to 8 line decoders (type 74als138). One of the decoders is responsible for all access that require fetching data from the INTF board and the other is responsible for the accesses that require the INTF board to receive data from the VME backplane.

A. EEPROM

There exists on the INTF board a 2k x 8 EEPROM which is used to store critical information that is specific to the particular module. From a practical point of view this EEPROM is no different than any other memory that could have been accessible to the VME backplane with the exception that the contents of the EEPROM is not lost when power is not applied.

B. FRONT PANEL I/O

The front panel I/O can be divided into three distinct areas. They are

1. front panel buttons
2. front panel LEDS (lights)
3. front panel pots and probe selection

1. FRONT PANEL BUTTONS

The circuitry to allow the VME backplane to read the status of the front panel buttons is made up by using three octal inverting buffers (type 74als540) and three hex switch debouncers (type MC14490). There are also five signals that are readable by the VME backplane through this circuitry that do not come from buttons and therefore do not require debouncing. They are overload and PLL lock indicators from the ADC board. As far as the VME backplane is concerned, these three buffers are just read only ports on its address map. The need for switch debouncing is because of the digital noise caused at the moment a button is either depressed or released.

2. FRONT PANEL LEDS

The circuitry to allow the VME backplane to illuminate the front panel LED's is made by using four octal inverting latches (type 74als576) and one PAL (type 22v10) As far as the VME backplane is concerned this circuitry is simply five write only ports on its address map. The need to replace one of the octal latches with a PAL was to provide for the feature which would initialize the front panel with all of its lights off when the module is first powered up.

3. FRONT PANEL POTS and PROBE SELECTION

The circuitry to allow the VME backplane to read the status of the front panel pots is made by using two eight channel 8 bit analog to digital converters (ADC) (type MAX161). These ADC's continuously scan the present position of all the pots on the front panel and store in an internal dual port memory the digital equivalent. As far as the VME backplane is concerned the internal dual port memory are just 16 ports of read only memory just like the front panel buttons described above. There are actually only 10 pots on the front panel and 4 of the remaining ports are used to sense the type of probe if any that is attached to the plug-in. This is done by measuring the voltage of a voltage divider that is created when a probe is attached. Since the output of the voltage divider will vary as a function of the probe type, the VME is capable of determining the probe type. We have now accounted for 14 out of the 16 possible ports that are available in these 2 ADC's. The remaining 2 ports are spares. There are two remaining pieces of circuitry associated with the ADC's. One is a dual operational amplifier (op amp type LM358) which is used to create the voltage references needed for the ADC circuitry. This circuit generates a heavily filtered +5 volt reference which goes to both the front panel as an input to all front panel pots and the other half of the dual op amp which simply inverts the +5 to create the -5 volt reference needed by the ADC's. The second circuit is a quad op amp (type LM324) which simply buffers the probe inputs prior to the ADC's.

C. VME STATUS/CONTROL REGISTERS

There are two registers which allow the VME backplane to provide direct communication between itself and various parts of the plug-in module. The status register is a 10 bit read only port (type 74als29827) which allow the VME backplane to monitor various parameters about the present status of the plug-in. Refer to the module plug-in specification for detailed description of the contents and the meaning of the individual bits within the status register. The control register is a 9 bit write only register (type 74als29823) which control certain functions of both the INTF board and the ICON interface. Again refer to the module plug-in specification for detailed description of the contents and the meaning of the individual bits within the control register.

4.3.2.4. VME SECTION (GLOBAL BUS INTERFACE)

The communication between the VME backplane and the resources of the global bus is through a set of address and data buffers. Remember from above, any access by the VME backplane to the global bus requires the VME interface controller to first request service from the global bus arbitor before it can

continue with its transfer. Once the global bus arbitor has granted the VME backplane access to the global bus, the VME address lines along with its data and write strobes are transferred onto the global bus address lines through three octal non-inverting buffers (type 74als541). Also the VME data bus is routed onto the global data bus through two octal transceivers (type 74als645). The global bus arbitor then informs the VME interface controller that the transfer has been completed so that the VME interface controller can terminate the transfer cycle to the backplane assuming that the transfer cycle was not a long (32 bit) type which would require the VME interface controller to initiate a second transfer request with the address lines incremented by 1 before terminating the backplane cycle.

4.3.2.5. VME SECTION (VME INTERRUPT HANDLER/CONTROLLER)

The VME interrupt handler/controller is 1 PAL which will monitor any interrupt requests from either TMS processor and perform the correct VME interrupt request protocol including prioritization.

4.3.2.6. TMS PROCESSOR SECTION (LOCAL RESOURCES)

A. UVPROM
Each TMS processor has 32k x 16 of UVPROM for storage of reset and interrupt vectors.

B. LOCAL MEMORY
Each TMS processor has 32k x 16 of static memory which under program control cab be shared as both program or data memory.

C. STATUS/CONTROL REGISTERS
Each TMS processor has a 16 bit control register to pass information between itself and the other TMS plus the VME backplane and the ICON interface. Each TMS processor has a 16 bit status register to monitor information between itself and the other TMS plus the VME backplane and the ICON interface.

D. MIN/MAX GATE ARRAY
Each TMS processor has a LeCroy designed gate array for calculation of MIN/MAX peak peaking routines.

E. PAGE REGISTERS
Each TMS processor has two 8 bit page registers to allow it to access all the resources of the global bus. Note that the combined resources of the global bus requires more addressability than the TMS has available so that a paging

scheme is necessary. By having 2 page registers, block memory moves between any two addresses becomes a lot more efficient.

F. VME INTERRUPT REQUEST REGISTER

Each TMS processor has an 8 bit register which it can set a VME interrupt vector into. By writing to this register an VME interrupt level 4 will be generated and the TMS will be informed when it's interrupt has been serviced by the VME backplane.

4.3.2.7. TMS PROCESSOR SECTION (GLOBAL BUS INTERFACE)

The interface between the TMS processor and the global bus is the same as the VME interface to the global bus except that the address lines for the global bus is a combination of 13 address lines from the TMS processor plus 8 bits of the selected page register.

4.3.2.8. GLOBAL BUS SECTION (BUS ARBITOR)

The global bus arbitor simply acts like a traffic cop between the two TMS processors and the VME backplane in terms of who gets the global bus at any one time.

4.3.2.9. GLOBAL BUS SECTION (GLOBAL MEMORY)

The global memory is a 256k x 16 static memory array which can be accessed by any one of three sources. The memory array is constructed using 32k x 8 SRAM's in dual in-line packages.

DISASSEMBLY

5.0 INTRODUCTION

This section includes the instrument disassembly and replacement procedures.

Note: Refer to table 5.0 for the correct board type for the version of module being repaired.

> WARNING DISASSEMBLY DESCRIBED IN THIS SECTION IS PERFORMED WITH POWER REMOVED FROM THE INSTRUMENT. DO NOT REMOVE OR REPLACE ANY OF THE CIRCUIT BOARD ASSEMBLIES WITHOUT FIRST VERIFYING THAT POWER HAS BEEN REMOVED FROM THE INSTRUMENT
>
> ANTI-STATIC PROTECTION MEASURES SHOULD BE TAKEN PRIOR TO THE HANDLING OF ANY PRINTED CIRCUIT BOARDS!

5.1 MODULE COVER REMOVAL

1. Referring to Fig. 5.1, remove the four short screws labeled B holding the front panel to the top cover of the module.
2. Remove the two screws labeled A on each side of the cover near the center of the bottom rail of the module.
3. Remove the two screws labeled C holding the rear plate assembly to the cover.
4. Remove the two screws labeled D holding the rear plate to the bottom rail of the module.
5. Loosen but do not remove the four long screws labeled E through the bottom rail of the module.
6. Carefully slide the front panel past the probe rings on the front of the module.
7. With one hand grasp the top center of the housing cover and with the other hand hold the bottom rail firmly to the table. Pull the top cover off the module.

5.2 MODULE COVER REPLACEMENT

1. Place module housing on table with opening facing up.
2. Place module assembly into cover with the ICON down as shown in Fig. 5.1
3. Install front panel and bottom rail as described in Sect. 5.4.

5.3 FRONT PANEL REMOVAL

1. Place the plug-in module upside down as shown in Fig. 5.1 and remove the four short screws labeled B that attach the front panel assembly to the housing.
2. Remove the four long screws labeled E through the bottom rail which attach to the 7242EXTR and the 7242AMP.
3. Remove the two screws labeled D which attach the rear bracket to the bottom rail.
4. Remove the two screws labeled A on each side of the module which attach the bottom rail to the cover.
5. Pull up rail assembly and remove from module.
6. Gently pull the front panel off of the module, being careful to avoid damaging the probe rings around the CH1, CH2 and External Trigger BNC connectors.

5.4 FRONT PANEL REPLACEMENT

1. Carefully slide front panel past probe rings and probe ring wires, and connect the connector which mates with the INTF board. Care must be taken so that the nylon housing around the probe ring does not get crushed by the front panel. Move the front of the AMP and the EXTR from side to side so that the front panel mates properly with the probe ring housings.
2. Install four short screws labeled B which attach front panel to housing.
3. Install bottom rail assembly by holding rail at an angle engage the rear edge of the boards into the slots in the rail. Exert firm pressure against the back of the rail so the boards do not disengage from it and gently rock the rail from side to side while lowering it in the front. When the rail is almost touching the boards toward the front align the boards through the hole in the bottom of the rail so that they are all engaged properly into the slots in the rail.
4. Reinstall four screws labeled A,(two on each side), which hold the housing to the rail.
5. Reinstall two screws labeled D into the back of the rail which secure the rear plate to the rail.
6. Reinstall the four long screws labeled E through the bottom of the rail into the AMP and EXTR.

5.5 FRONT PANEL DISASSEMBLY

1. Perform the front panel removal procedure of Sect. 5.3.
2. Using a fingernail or a thin bladed knife, pry caps off of Timebase, Trigger Level, Trigger Delay, Var. Gain and Offset knobs as shown in Fig 5.3.
3. Use screwdriver to loosen screws inside knobs one half turn counterclockwise, then remove knobs.
4. Use a nut driver or needle nose pliers to loosen the nut in the center of the Volts/Div. knob, then remove knob.
5. From rear of front panel remove 7 Phillips head screws and split washers to remove 7242FPCB assembly from front panel.

5.6 FRONT PANEL ASSEMBLY

1. Reverse the disassembly procedure to reassemble the front panel. Note that the knob on the Var. V/Div. is slightly smaller than the other three small knobs. Sufficient clearance should be allowed between all knobs and the front panel, and between the Var. V/Div. knob and the V/Div. knob so that they do not bind when turned. When the small caps are reinstalled, note that the notch on the knob and the key way on the cap should be aligned.

5.7 EXTERNAL TRIGGER REMOVAL

1. Perform the module cover removal (Sect 5.1).
2. Place the module upside down on the table (7242ICON down).
3. Remove tape from side of 7242EXTR assembly and disconnect white wire that connects J1 to the INTF assembly.
4. Disconnect P9 and P10 from TMB assembly as shown in Fig 5.2.
5. Disconnect cable end J3 from TMB assembly and remove EXTR from module.

5.8 EXTERNAL TRIGGER REPLACEMENT

1. Connect ribbon cable to EXTR so that red wire on ribbon cable is towards rear of the EXTR (the end opposite the BNC connector) and so that the cable crosses over the EXTR board.
2. Place EXTR in location on side of module on top of the ADCA board. Connect free end of ribbon cable to TMB.
3. Dress coax cables so that they are between ADCA and TMB board and that they go over top of the two coaxes that connect to the ADCA board. Connect P9 and P10 to the TMB. J9 is labeled EXT* and J10 is labeled EXT on the TMB.
4. Reconnect white wire from J3 of INTF to J1 on probe ring. Secure with adhesive tape on the side of the EXTR shield.
5. Perform the module cover replacement procedure (Sect 5.2).

5.9 AMPLIFIER BOARD REMOVAL

1. Perform the module cover removal (Sect 5.1).
2. Place the module upside down on the table (7242ICON down).
3. Remove tape from side of 7242AMP assembly and disconnect white wire that connects J1 and J5 to the INTF assembly.
4. Disconnect P5, P6, P7 and P8 from TMB assembly, P1 and P2 from ADCA assembly.
5. Separate AMP/TAMP assembly from the TMB board by using connectors J1 and J2 to lift AMP assembly slightly, then insert one finger between the TMB and MEM boards and use a gentle, but firm rocking and lifting motion to disconnect TAMP assembly from connectors P1 and P2 on upper edge of TMB board.
6. Push MEM and TMB boards apart slightly and remove TAMP and AMP assemblies, being careful to guide wires disconnected in step 4 around twisted pairs spools on TMB board.

5.10 AMPLIFIER BOARD REPLACEMENT

Note: AMP and ADCA should be replaced as a set!

1) Place the 7242TAMP on the AMP with the caps near the edge of the TAMP facing towards the AMP.
2) Connect the TAMP and AMP to the TMB, placing the coax wires from the AMP in the space below the wire spools on the TMB.

3) Connect the cables from the AMP labeled P5 through P8 to the TMB with P5 connecting to the connector closest to the ICON (labeled CH1*) as shown Fig 5.2.
4) Connect the cables from the AMP labeled P1 and P2 to the ADCA with P1 connecting to the connector farthest from the ICON. Dress these wires so they lay in the narrow valley on the TMB between the connectors (P5-P8) and the PC board.
5) Connect the cables from the EXTR to the TMB so that they go over top of the cables installed in step 4. Connect them so the connector labeled P9 is next to P8.
6) Reconnect white wires from J1 of INTF to J1 on AMP and J2 of INTF to J5 on AMP. Secure with adhesive tape on the side of the AMP shield.
7) Perform the module cover replacement procedure (Sect 5.2).

5.11 ANALOG TO DIGITAL CONVERTER (ADCA) BOARD REMOVAL

Note: AMP and ADCA should be replaced as a set!

1) Perform the module cover removal procedure (Sect 5.1).
2) Disconnect two cables from AMP labeled P1 and P2 from the front of the ADCA board.
3) Disconnect two cables from MEM labeled P3 and P4 from rear of ADCA.
4) Lift EXTR assembly up and out of the way, then insert a screwdriver in between the VME connectors on the ICON board and gently pry ADCA board up and out of connectors J14, J24, J34 and J44 to remove.

5.12 ANALOG TO DIGITAL CONVERTER (ADCA) BOARD REPLACEMENT

Note: AMP and ADCA should be replaced as a set!

1) Install ADCA by reversing the steps in section 5.11.
2) Temporarily place front panel and bottom rail on module and insert into Slot A of mainframe.
3) Perform ADCA timing adjustments in accordance with the procedure of Sect. 3.2.

5.13 MEMORY (MEM) BOARD REMOVAL

1) Perform the module cover removal procedure (Sect 5.1).
2) Disconnect three white wires from AMP and EXTR labeled P1, P2 and P3 from the INTF board.

3) Disconnect two cables from MEM labeled P3 and P4 from rear of ADCA.
4) Insert a screwdriver in between the VME connectors on the ICON board and gently pry INTF board up and out of connectors J11, J21, J31 and J41 to remove.
5) Disconnect two coax cables from MEM to ADCA and two coaxes form MEM to TMB.
6) Insert a screwdriver in between the VME connectors on the ICON board and gently pry MEM board up and out of connectors J12, J22, J32 and J42 to remove.

5.14 MEMORY (MEM) BOARD REPLACEMENT

1) Install MEM be reversing the steps in section 5.13.
2) Temporarily place front panel and bottom rail on module and insert into Slot A of mainframe.
3) Perform ADCA timing adjustments in accordance with the procedure of **Sect. 3.2**.

5.15 TIMEBASE (TMB) BOARD REMOVAL

1) Perform the module cover removal procedure (Sect 5.1).
2) Perform the AMP removal procedure (Sect. 5.9).
3) Perform the EXTR removal procedure (Sect. 5.7).
4) Disconnect two coax cables from MEM to ADCA and two coaxes form MEM to TMB.
5) Insert a screwdriver in between the VME connectors on the ICON board and gently pry ADCA board up and out of connectors J14, J24, J34 and J44 to remove.
6) Insert a screwdriver in between the VME connectors on the ICON board and gently pry TMB board up and out of connectors J13, J23, J33 and J43 to remove.

5.16 TIMEBASE (TMB) BOARD REPLACEMENT

1) Install TMB by reversing the steps in section 5.13.
2) Temporarily place front panel and bottom rail on module and insert into Slot A of mainframe.
3) Perform ADCA timing adjustments in accordance with the procedure of **Sect. 3.2.**
4) Perform delay calibration procedure in accordance with the procedure of **Sect. 3.1.**

5.17 INTERFACE (INTF) BOARD REMOVAL

1) Perform the module cover removal procedure (Sect 5.1).
2) Disconnect three white wires from AMP and EXTR labeled P1, P2 and P3 from the INTF board.
3) Insert a screwdriver in between the VME connectors on the ICON board and gently pry INTF board up and out of connectors J11, J21, J31 and J41 to remove.

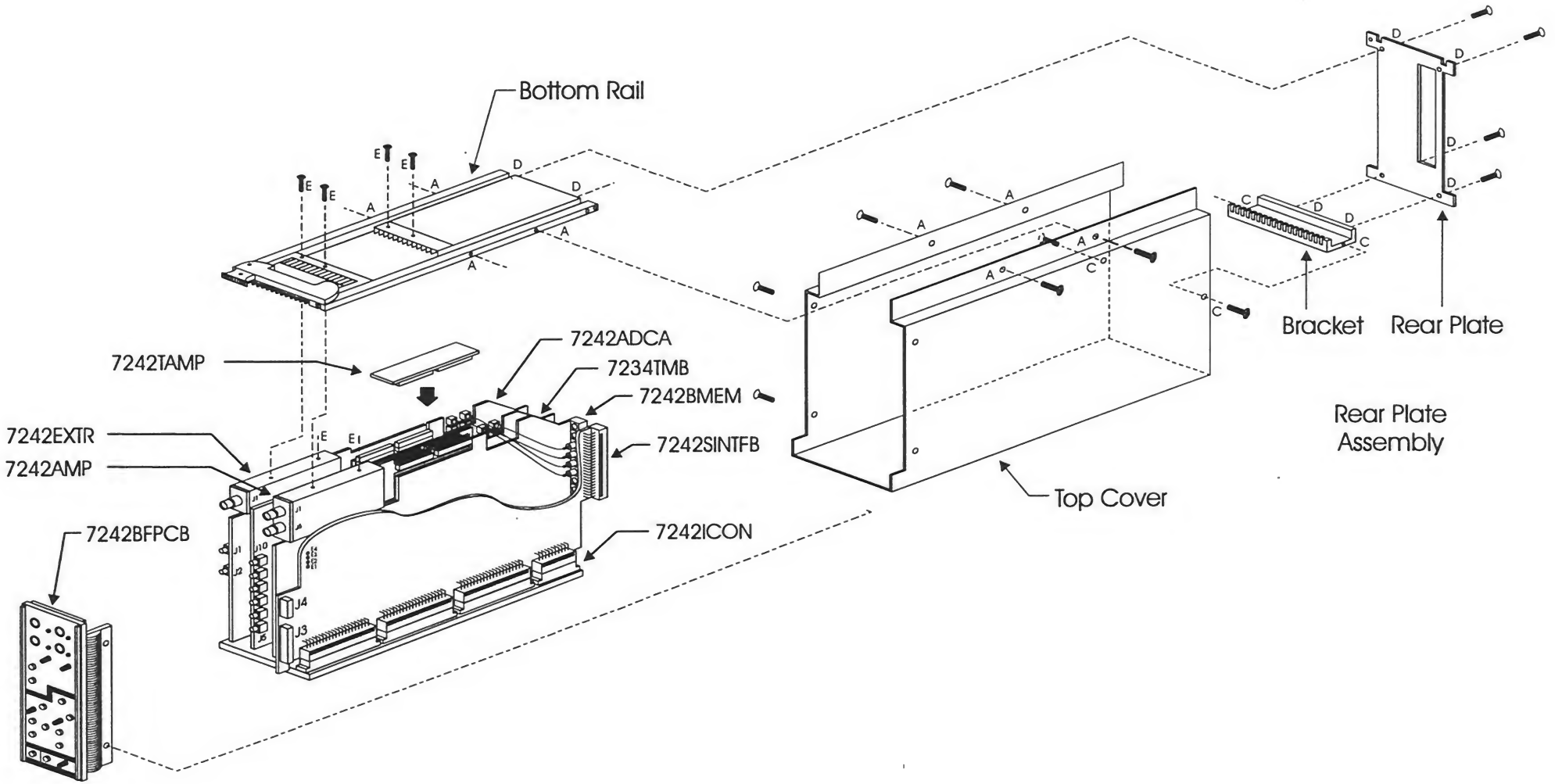
5.18 INTERFACE (INTF) BOARD REPLACEMENT

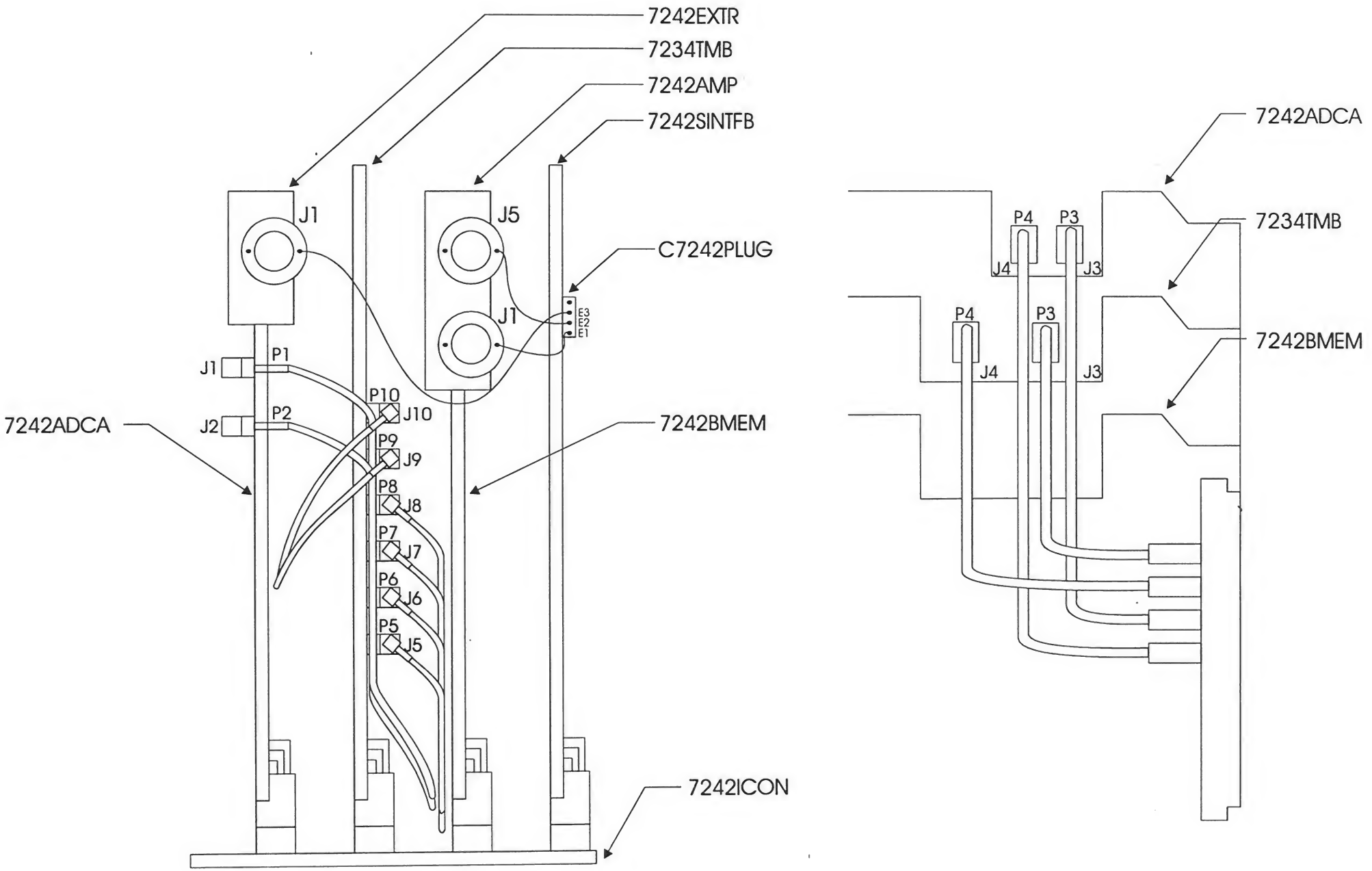
1) Install INTF be reversing the steps in section 5.17.
2) Perform delay calibration procedure in accordance with the procedure of **Sect. 3.1.**

	7242	7242A	7242B	7242B -L1	7242B -S1-L1	7234	7234-L1
7234ADC						*	*
7234AMP [1]						*	*
7234ICON						*	*
7234INTF [2]			*	*	*	*	*
7234MEM						*	
7234MEMA							*
7234TMB			*	*		*	*
7242ADC (REV C) [3,4]	*						
7242ADCA (REV C) [3,4]	*	*					
7242ADCA (REV D) [3]	*	*	*	*			
7242ADCA (REV E) [3]	*	*	*	*	*		
7242AMP [1]	*	*	*	*	*	*	*
7242BMEM			*				
7242BMEMA				*	*		
7242EXTR	*	*	*	*	*		
7242ICON	*	*	*	*	*		
7242INTF	*	*					
7242MEM	*						
7242MEMA	*	*					
7242SINTF					*		
7242SINTFA [2]			*	*		*	*
7242SINTFB [2]			*	*		*	*
7242TAMP	*	*	*	*	*	*	*
7242STMB					*		
7242TMB	*	*					

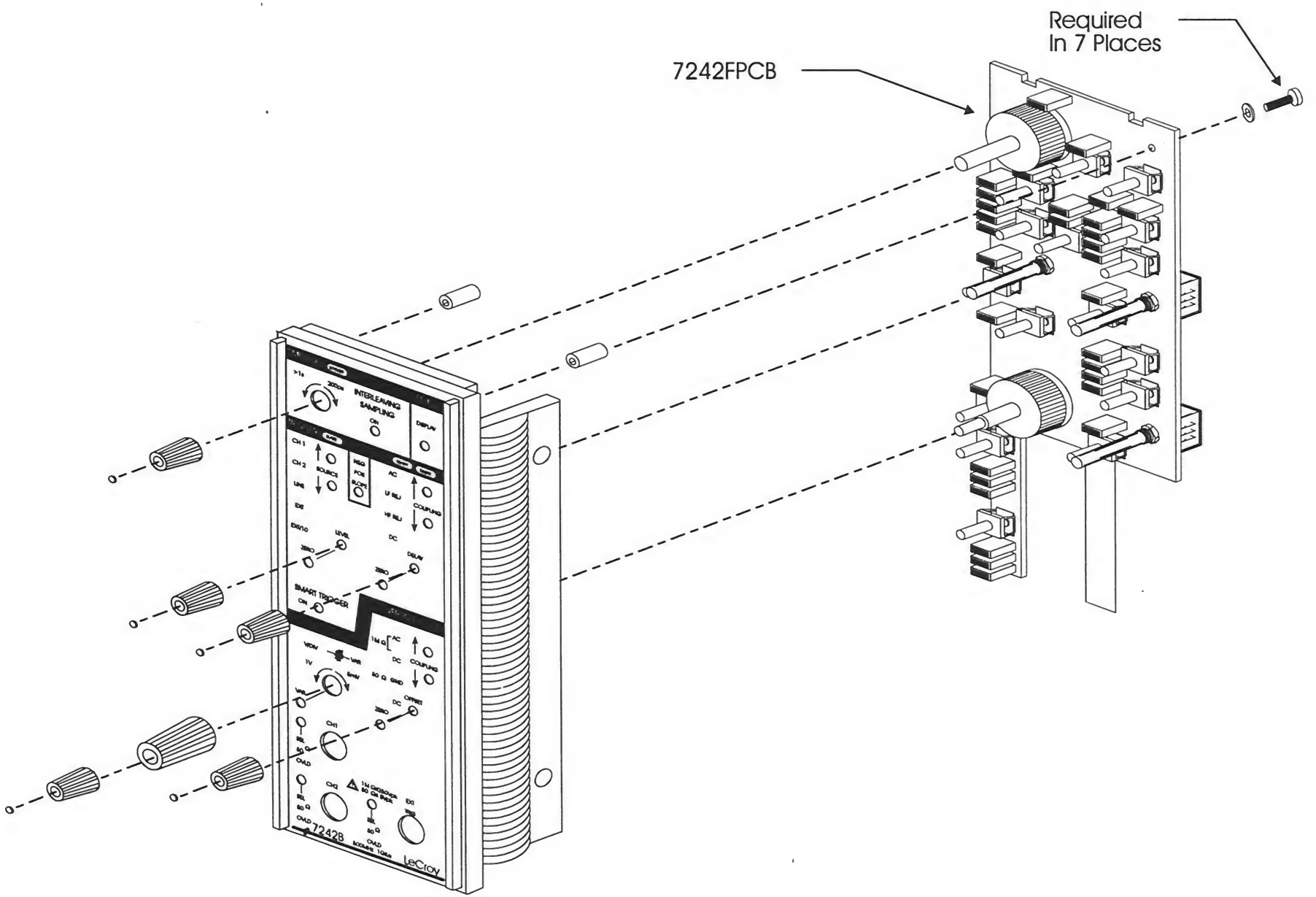
1 7242AMP and 7234AMP are shipped as sets with the appropriate ADC board.
2 7234INTF, 7242SINTFA and 7242SINTFB are interchangeable with one exception, the 7242SINTFB is the only board which supports the F-2 option.
3 Requires adjustment of memory timing signals.
4 Rev C boards have significant differences in delay lines depending on if their use will be as a 7242ADC or 7242ADCA.

TABLE 5.0

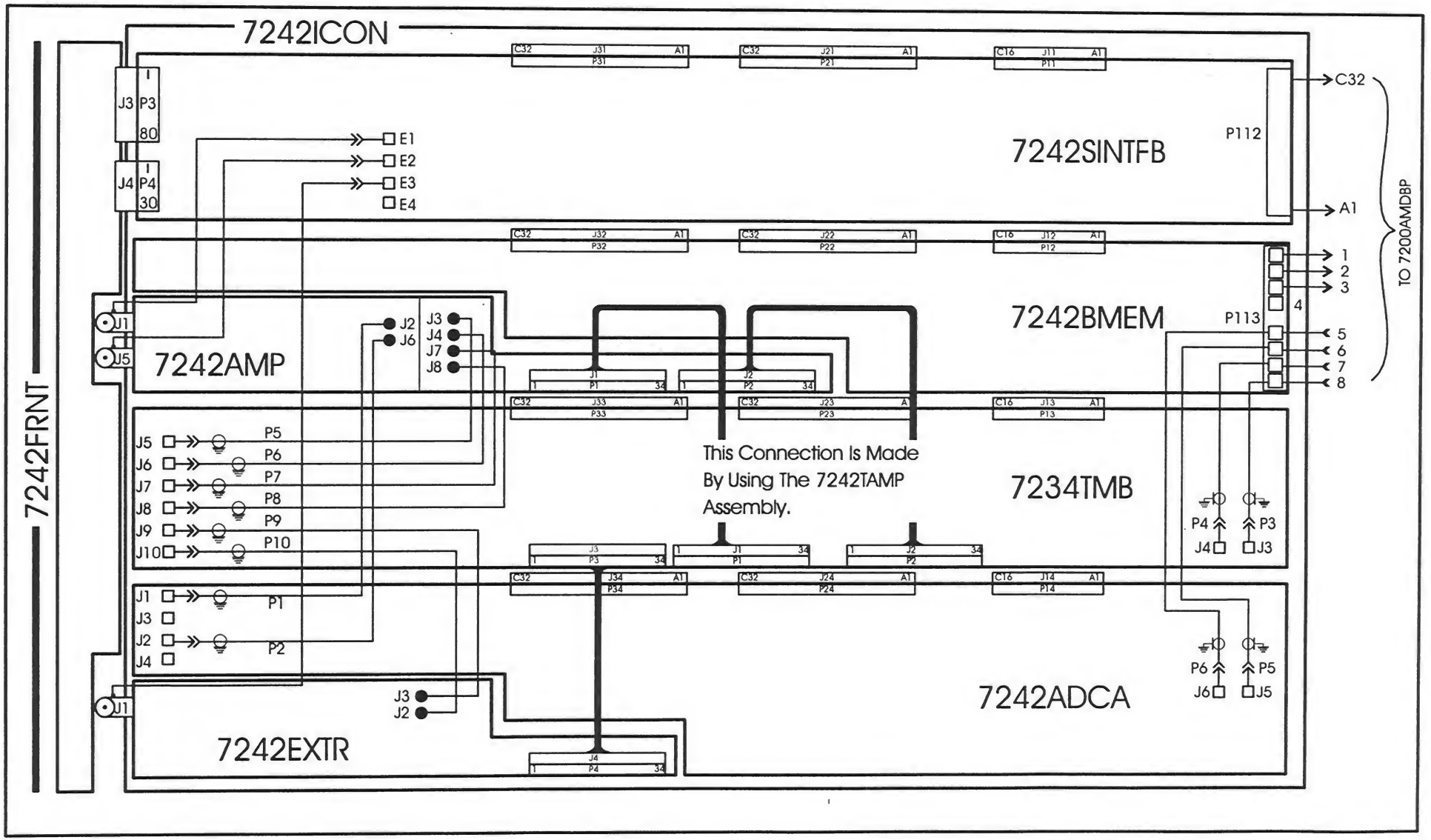

Bottom Rail
7242TAMP
7242ADCA
7234TMB
7242BMEM
7242SINTFB
7242EXTR
7242AMP
7242BFPCB
7242ICON
Top Cover
Bracket
Rear Plate
Rear Plate Assembly


7242EXTR
7234TMB
7242AMP
7242SINTFB
J1
J5
C7242PLUG
J1
E3
E2
E1
J1
P1
P10
J10
7242ADCA
J2
P2
7242BMEM
P9
J9
P8
J8
P7
J7
P6
J6
P5
J5
7242ICON
7242ADCA
7234TMB
P4
P3
J4
J3
P4
P3
7242BMEM
J4
J3

7242B Front Panel Replacement



7242B Plug In Wiring Diagram



7242B Plug In Cable Placement

Cable Assembly	From	To
487-234-002	7242SINTFB-E1	7242AMP-J1
487-234-002	7242SINTFB-E2	7242AMP-J5
487-234-002	7242SINTFB-E3	7234AMP-J1
C7242EXTR	7242EXTR-J3	7234TMB-J9(P9)
C7242EXTR	7242EXTR-J2	7234TMB-J10(P10)
C7242AMP2	7242AMP-J1	7242ADCA-P1
C7242AMP2	7242AMP-J6	7242ADCA-P2
C7242AMP4	7242AMP-J3	7234TMB-P5
C7242AMP4	7242AMP-J4	7234TMB-P6
C7242AMP4	7242AMP-J7	7234TMB-P7
C7242AMP4	7242AMP-J8	7234TMB-P8
C7242MEMA	7242BMEM-P113-5	7242ADCA-J6(P6)
C7242MEMA	7242BMEM-P113-6	7242ADCA-J5(P5)
C7242MEMB	7242BMEM-P113-7	7234TMB-J4(P4)
C7242MEMC	7242BMEM-P113-8	7234TMB-J3(P3)
C7242EXTMB	7242EXT-J4(P4)	7234TMB-J3(P3)

Table 5.1

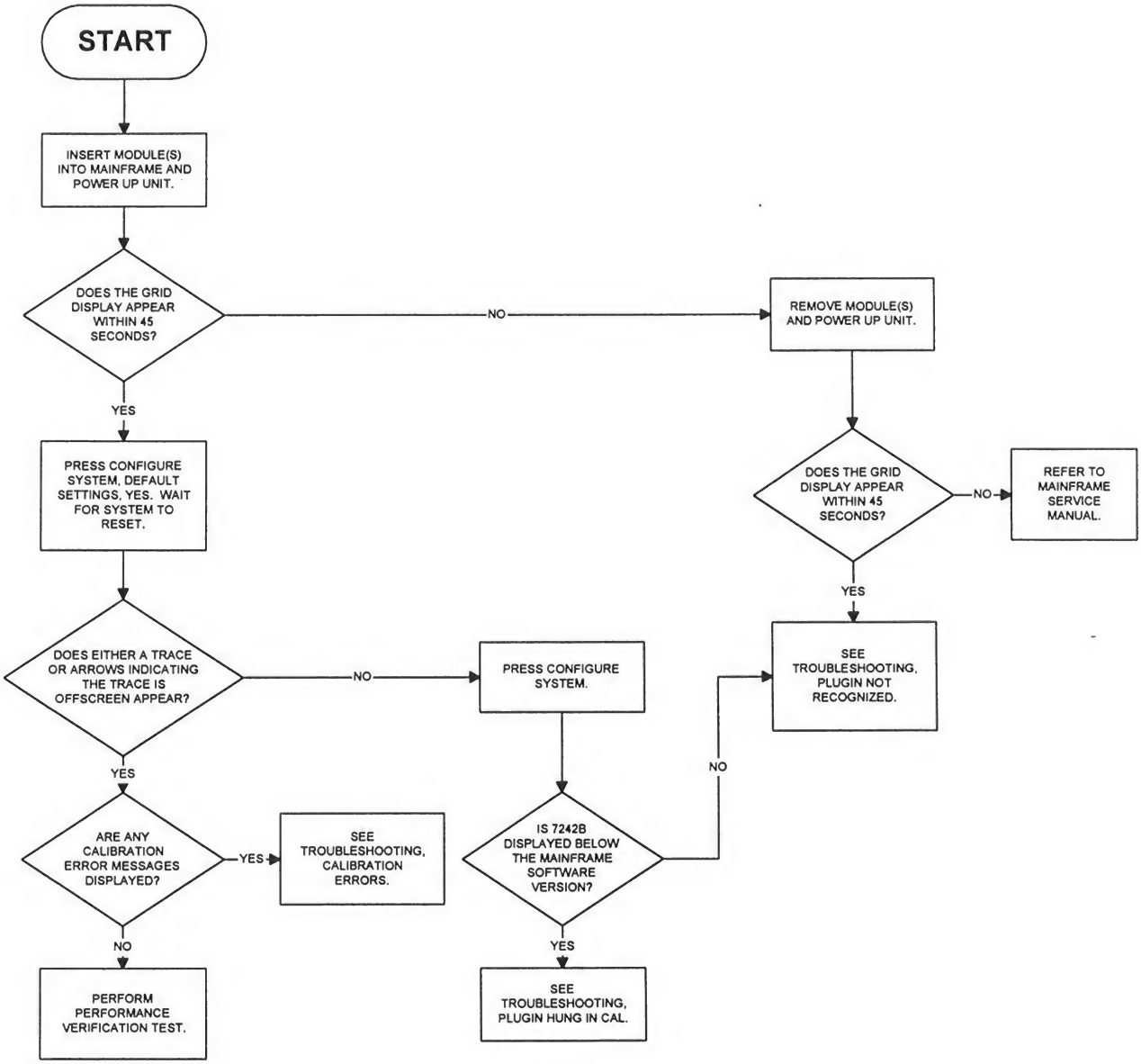
7242/A/B TROUBLESHOOTING

6.0 INTRODUCTION

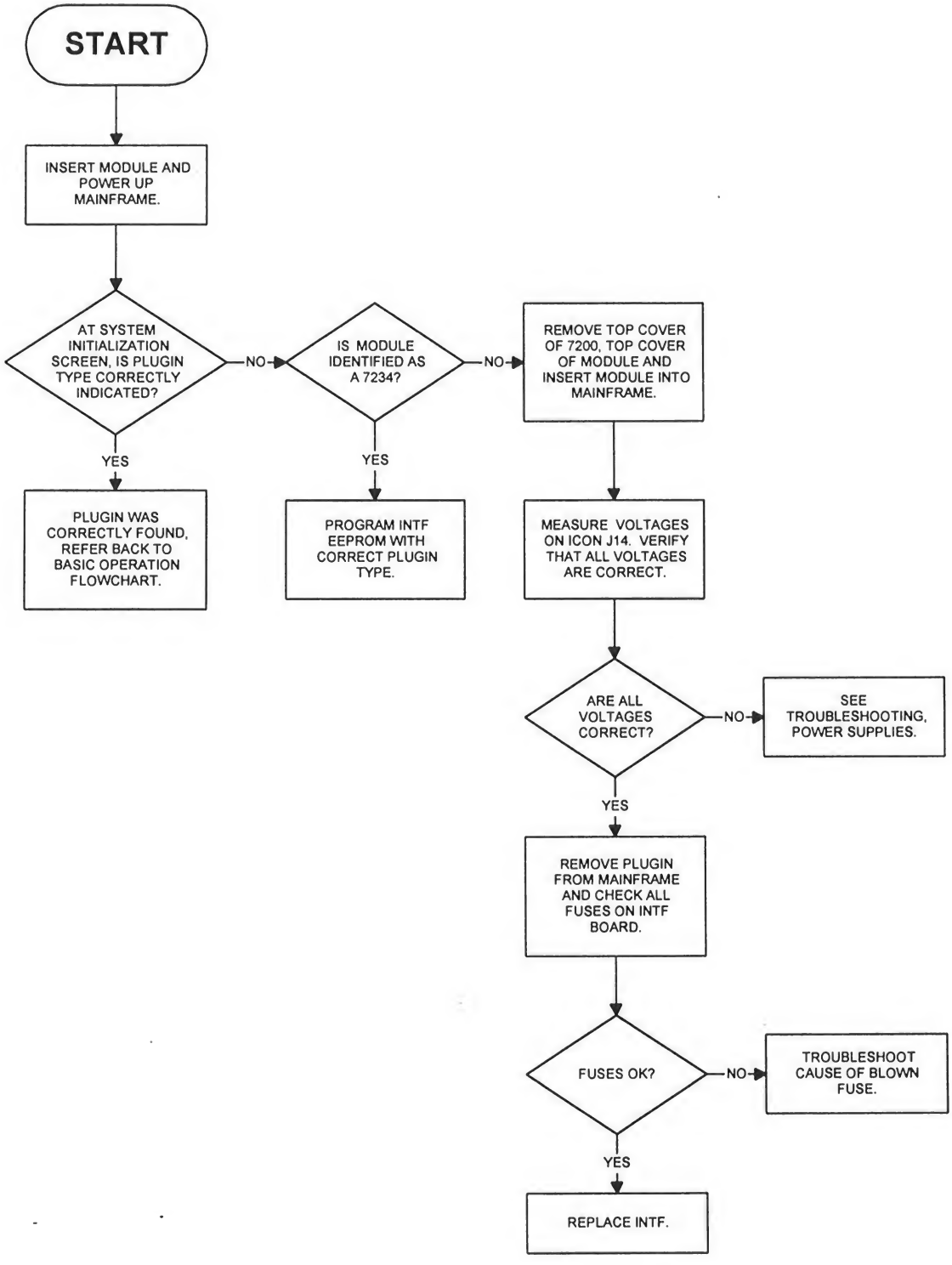
This section will guide service personnel in troubleshooting the 7242(A/B) Digitizing Module by the use of flow charts. The section is divided into 8 parts:

1. Basic Operation
2. Module not recognized
3. Calibration errors
4. Module does not trigger
5. Flyers
6. Plugin Hung in Cal
7. Power Supplies

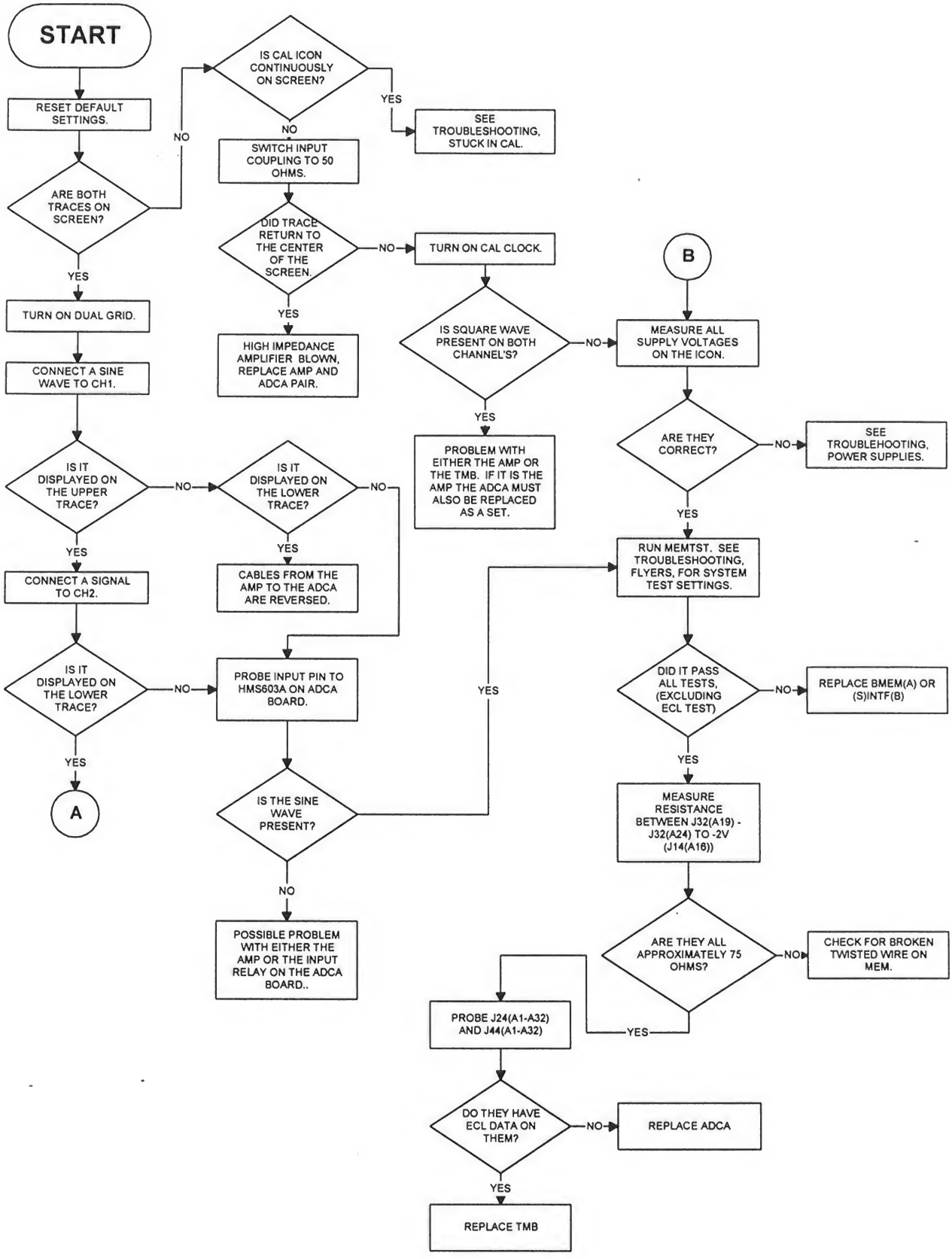
6.1 Basic Operation



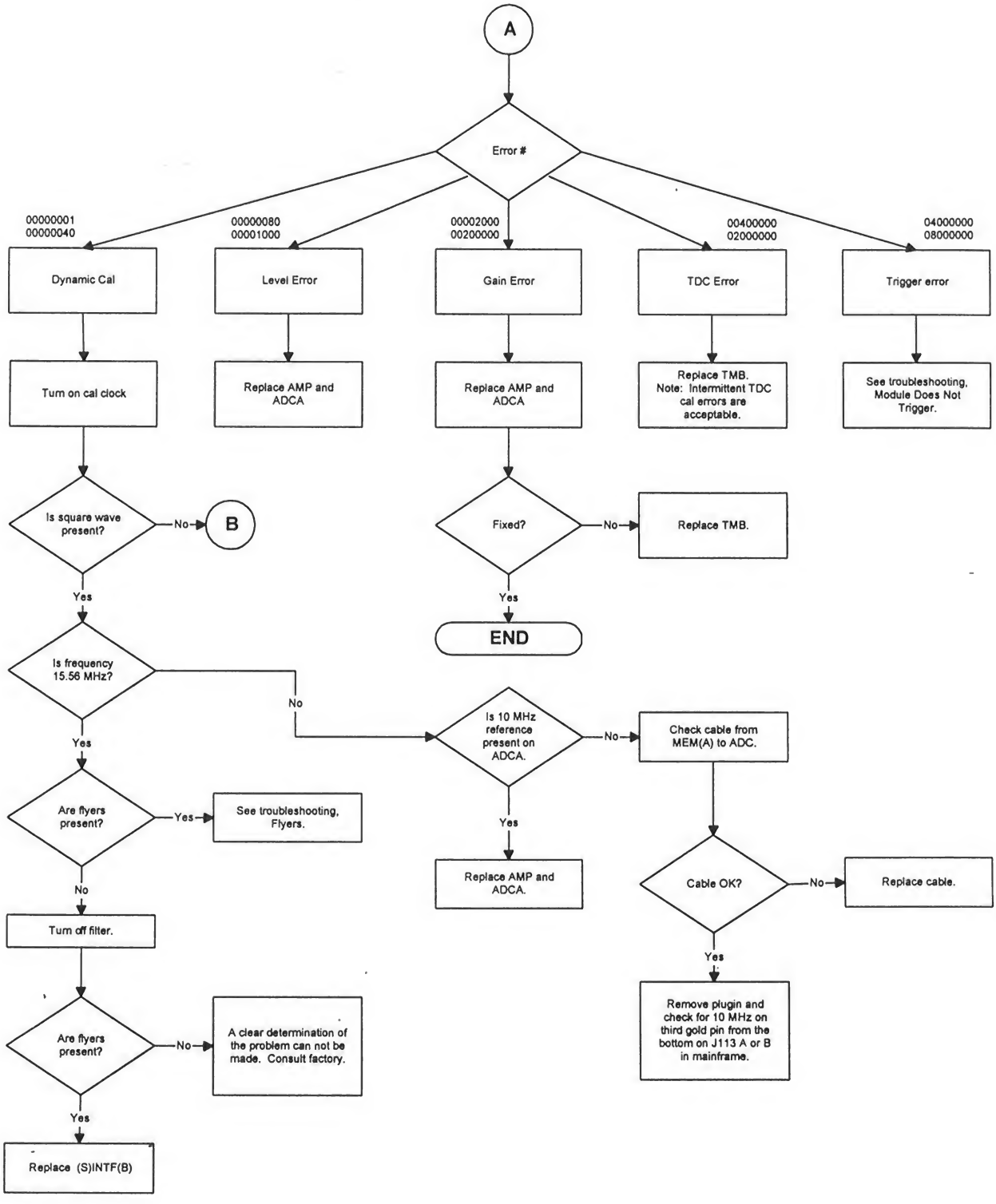
6.2 Module not recognized



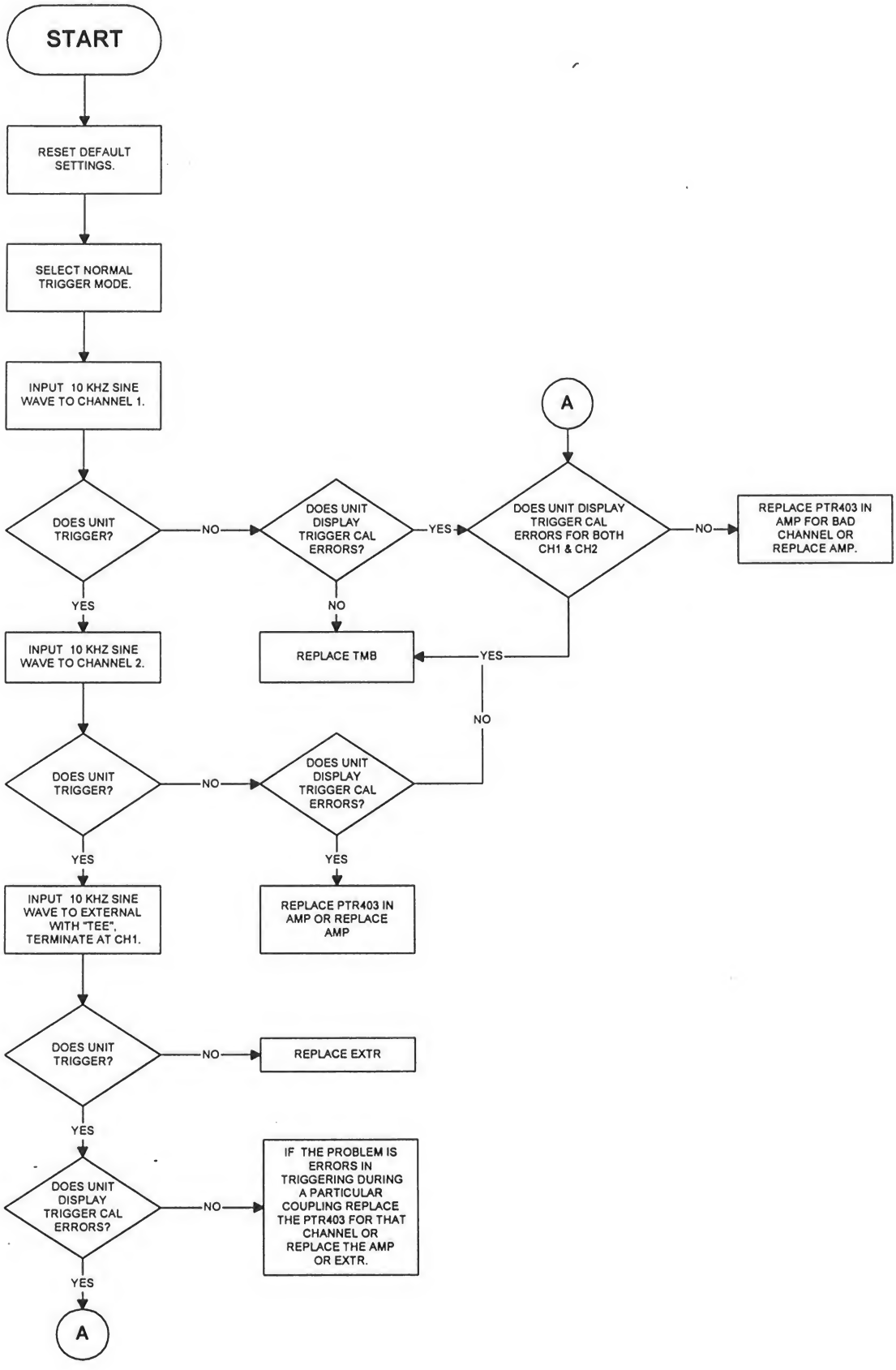
6.3 Calibration errors



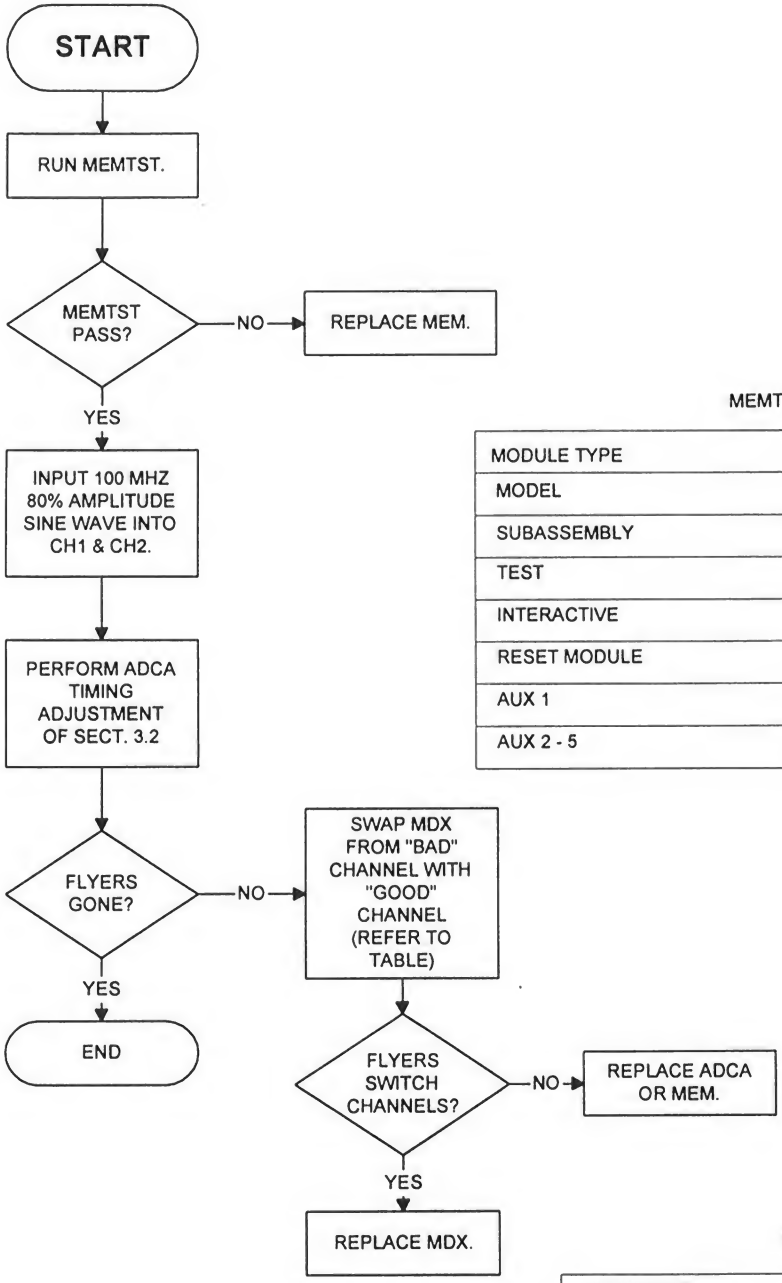
6.3 Calibration errors (cont'd)



6.4 Module does not trigger



6.5 Flyers



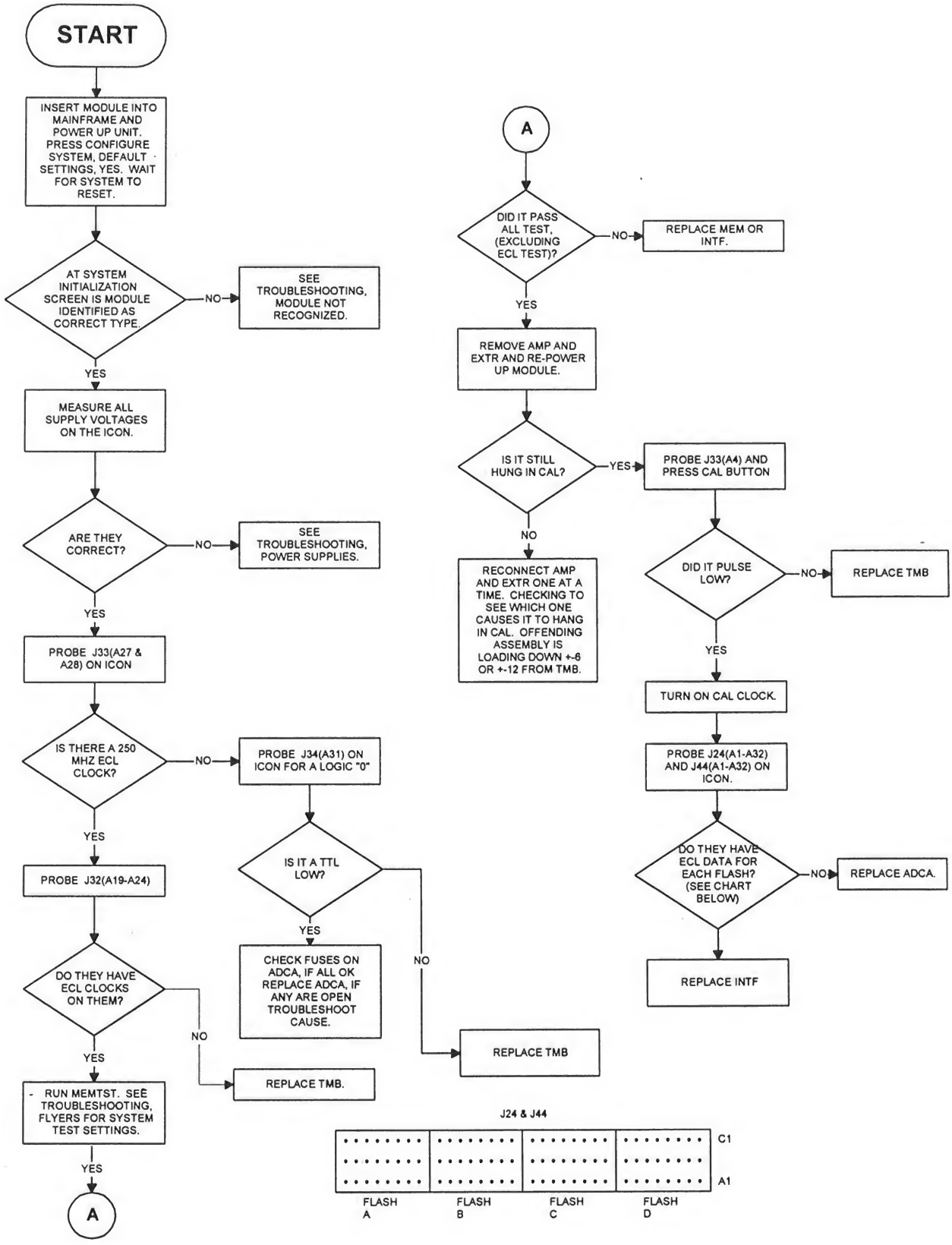
MEMTST SYSTEM TEST SETTINGS

MODULE TYPE	7242	7242B	7242B-L1	7234	7234-L1
MODEL	P42	P34	P34	P34	P34
SUBASSEMBLY	MEM	MEM	MEM	MEM	MEM
TEST	MEM7242	MEM7234	MEM7234	MEM7234	MEM7234
INTERACTIVE	YES	YES	YES	YES	YES
RESET MODULE	YES	YES	YES	YES	YES
AUX 1	0	0	1	0	1
AUX 2 - 5	0	0	0	0	0

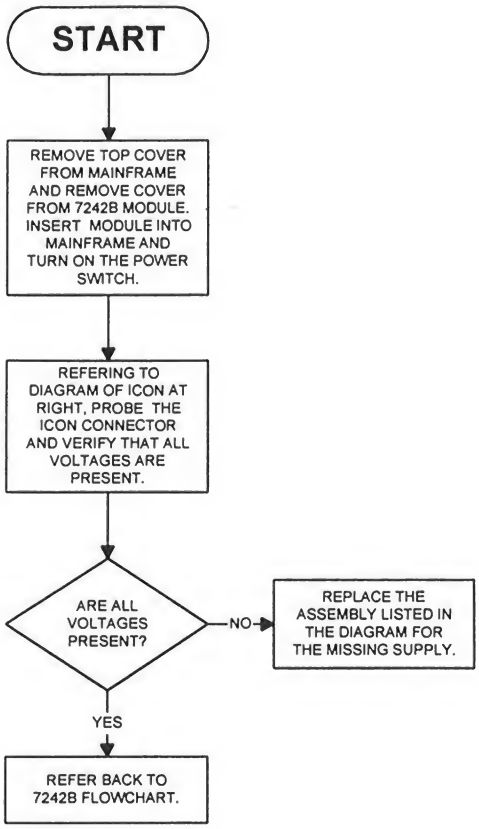
MDX LOCATION CHART

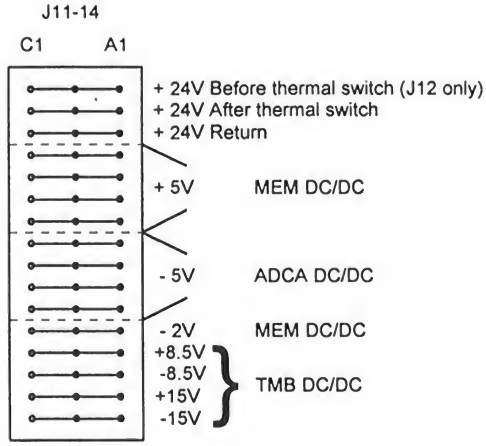
FLYER SIZE	BIT	CH1	CH2
4 MAJOR DIVISIONS	7	U3	U70
2 MAJOR DIVISIONS	6	U3	U70
1 MAJOR DIVISION	5	U17	U85
1/2 MAJOR DIVISION	4	U17	U85
1/4 MAJOR DIVISION	3	U31	U99
1/8 MAJOR DIVISION	2	U31	U99
1/16 MAJOR DIVISION	1	U45	U113
1/32 MAJOR DIVISION	0	U45	U113

6.6 Plugin Hung in Cal

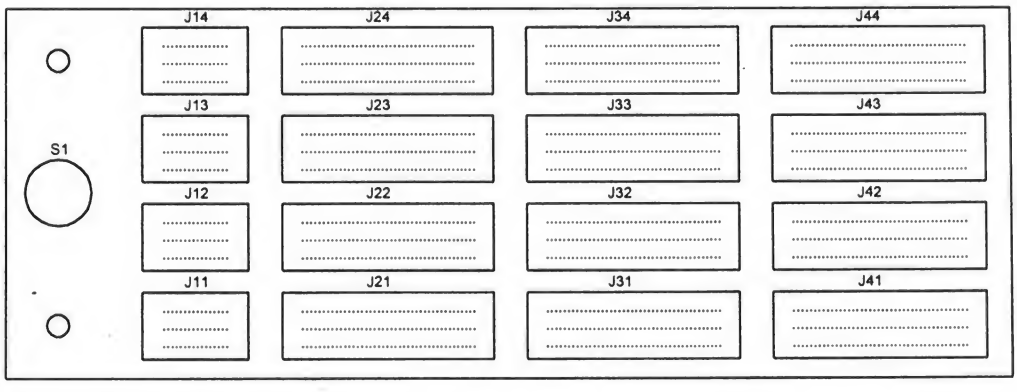


6.7 Power Supplies





7242ICON



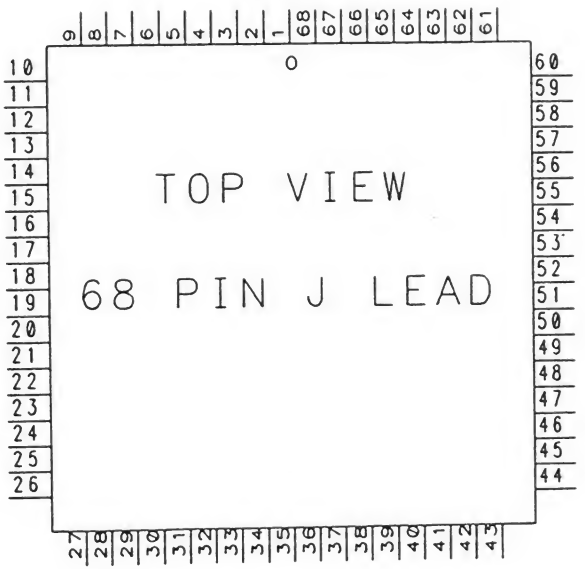
ICON TOP VIEW

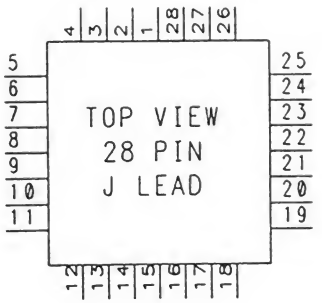
2	DAC
3	SH1
4	FLASH1
5	SH2
6	FLASH2
7	DATA
8	CLOCK
9	CLKDRIVE
10	CONNECT
11	POWER
12	DCDC

TIMING
LAYOUT
PARTS
TIMING

7242ADC MEMORY MAP

ADDRESS	LOWER BYTE FUNCTION	UPPER BYTE FUNCTION
40000000	CH1 FLASH A GAIN	CH1 COARSE S_H A OFFSET
40000004	CH1 FLASH B GAIN	CH1 FINE S_H A OFFSET
40000008	CH1 FLASH C GAIN	CH1 COARSE S_H B OFFSET
4000000C	CH1 FLASH D GAIN	CH1 FINE S_H B OFFSET
40000010	CH1 S_H A DELAY	CH1 COARSE S_H C OFFSET
40000014	CH1 S_H B DELAY	CH1 FINE S_H C OFFSET
40000018	CH1 S_H C DELAY	CH1 COARSE S_H D OFFSET
4000001C	CH1 S_H D DELAY	CH1 FINE S_H D OFFSET
40000020	CH2 FLASH A GAIN	CH2 COARSE S_H A OFFSET
40000024	CH2 FLASH B GAIN	CH2 FINE S_H A OFFSET
40000028	CH2 FLASH C GAIN	CH2 COARSE S_H B OFFSET
4000002C	CH2 FLASH D GAIN	CH2 FINE S_H B OFFSET
40000030	CH2 S_H A DELAY	CH2 COARSE S_H C OFFSET
40000034	CH2 S_H B DELAY	CH2 FINE S_H C OFFSET
40000038	CH2 S_H C DELAY	CH2 COARSE S_H D OFFSET
4000003C	CH2 FLASH D GAIN	CH2 FINE S_H D OFFSET





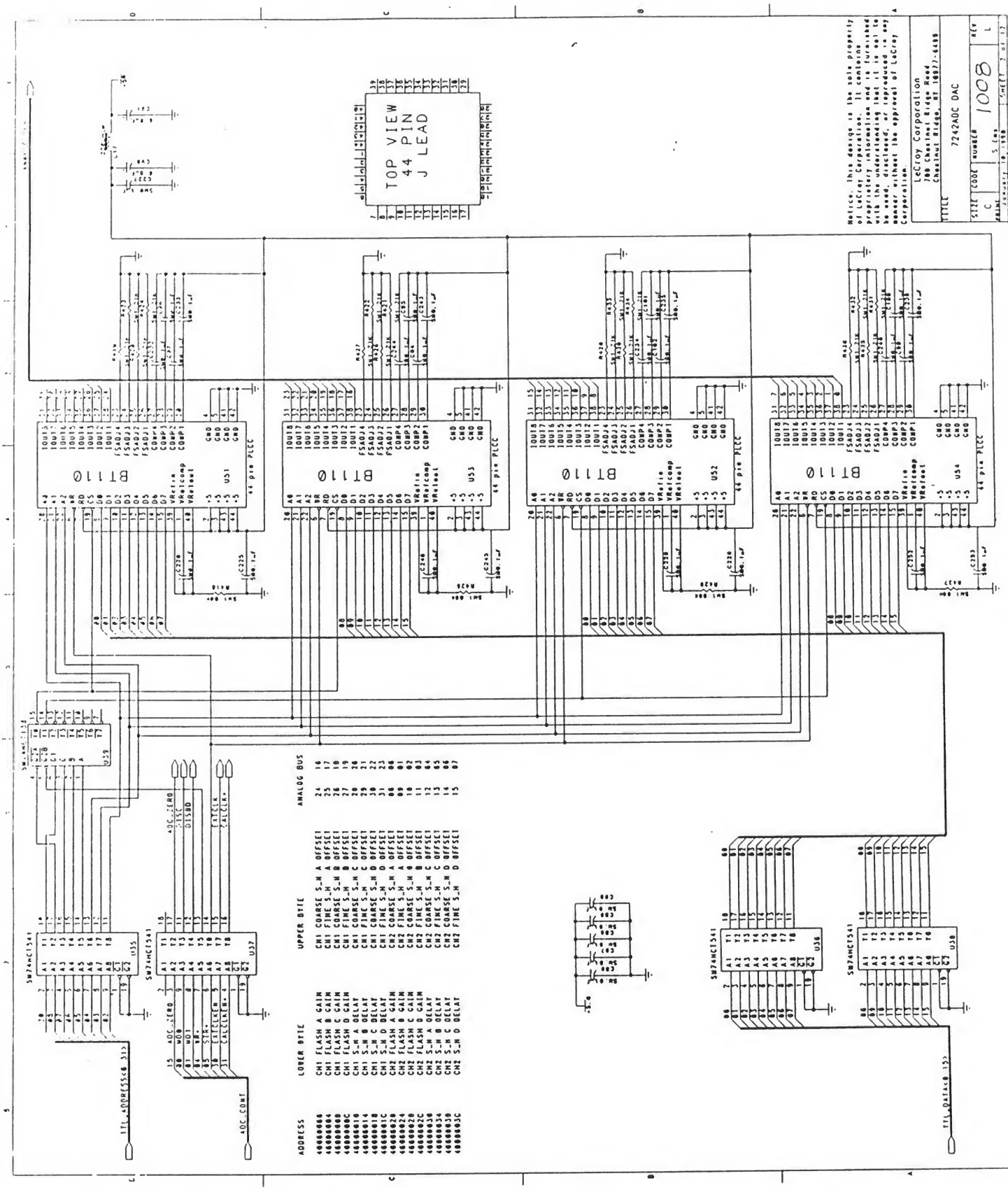
LeCroy Corporation
700 Chestnut Ridge Road.
Chestnut Ridge, NY 10977-6499

TITLE: 7242ADC TOP LEVEL

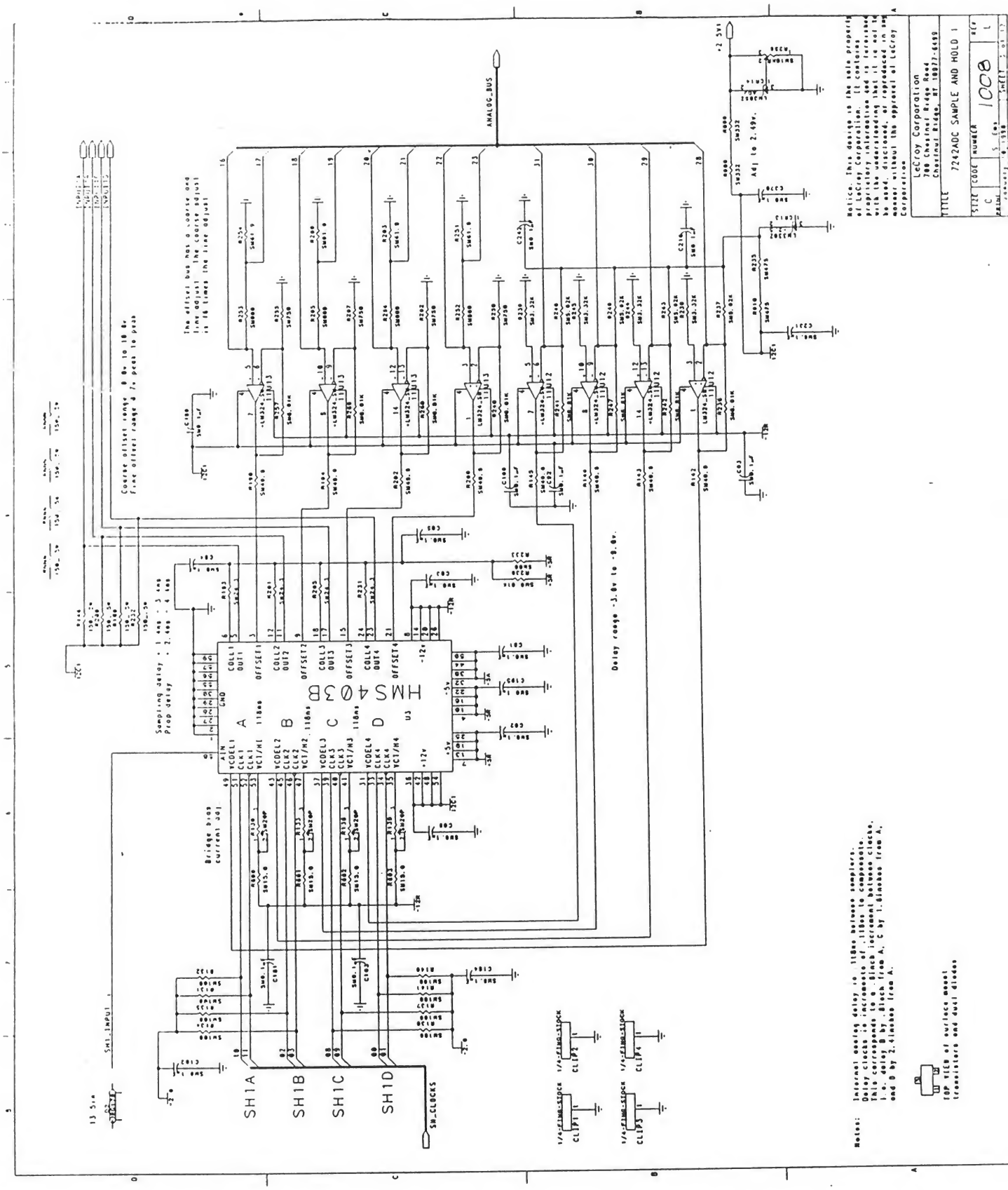
SIZE	CODE	NUMBER	REV
A		1008	L

PPINT: S. Ems

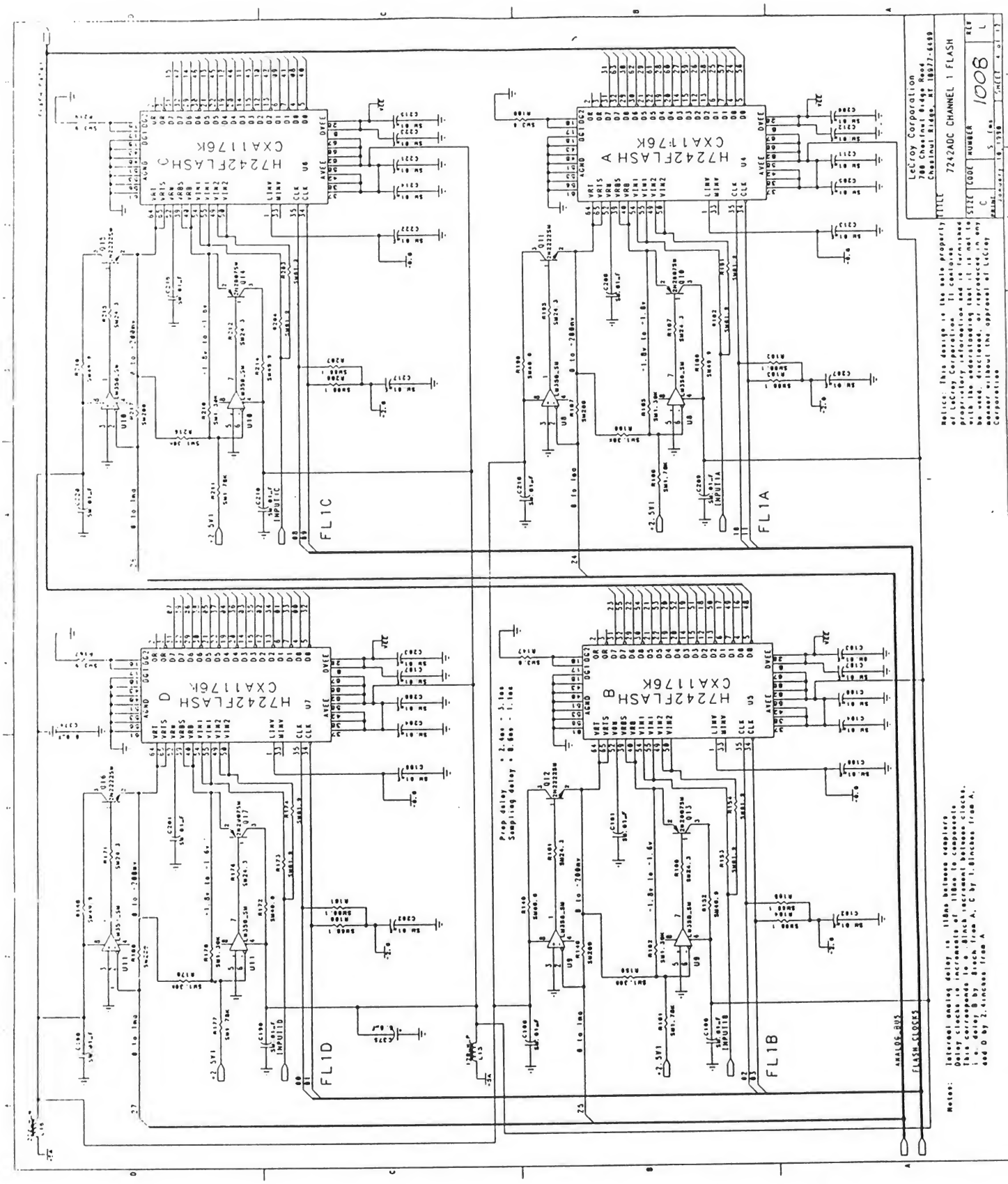
January 10, 1990 | SHEET 1 of 12



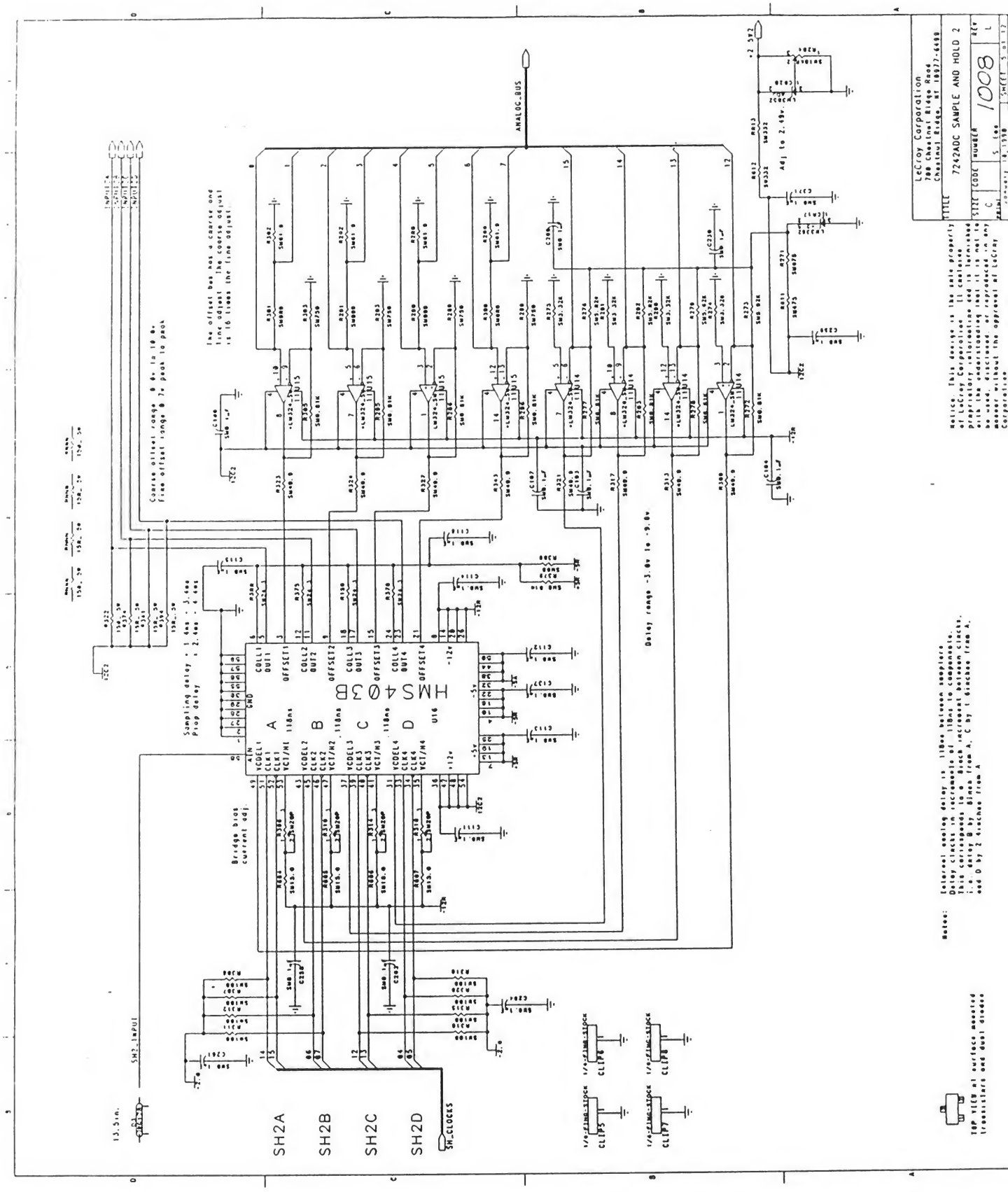
7242ADC **Sheet 2.**



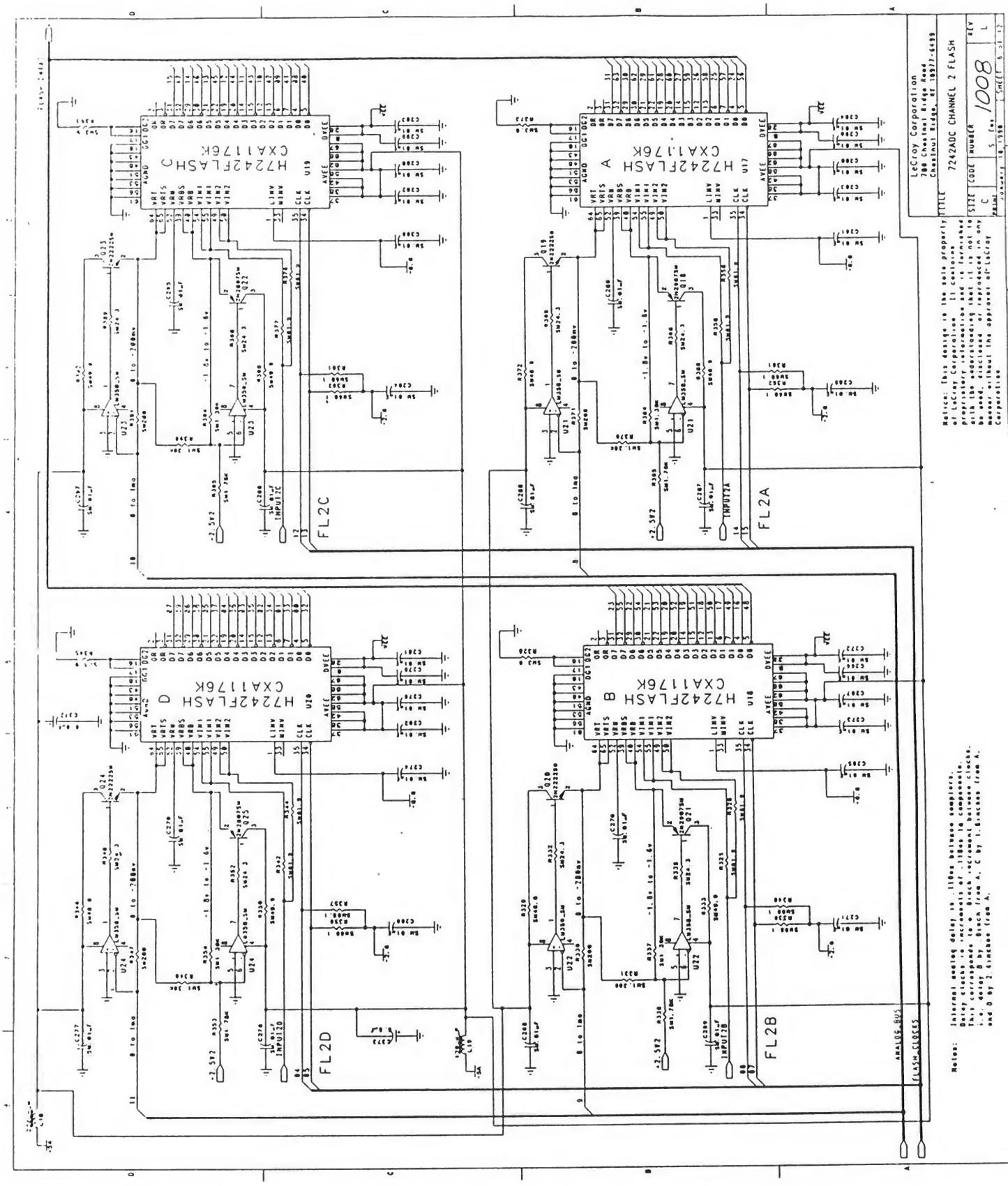
7242ADC **Sheet 3.**

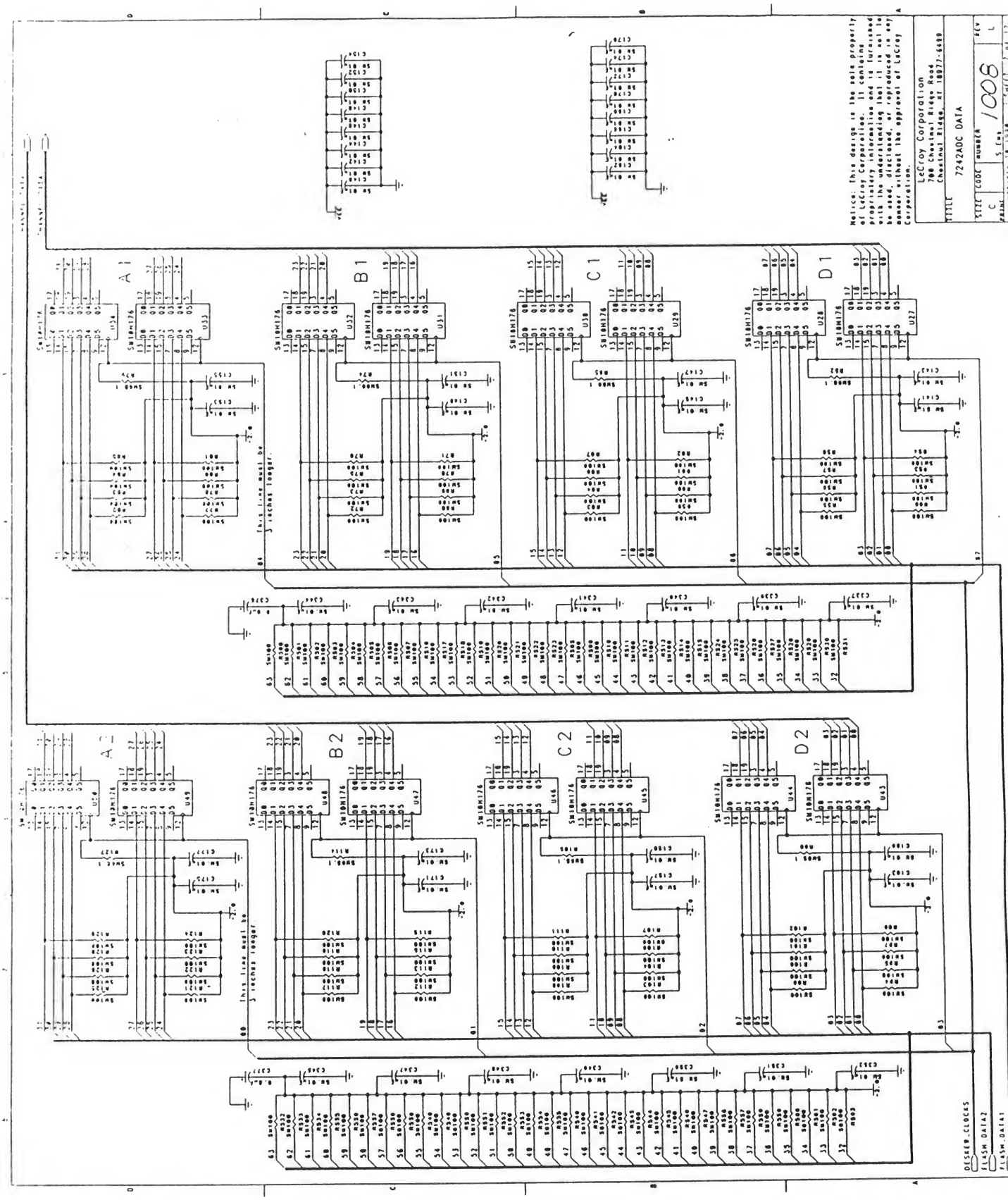


7242ADC **Sheet 4.**

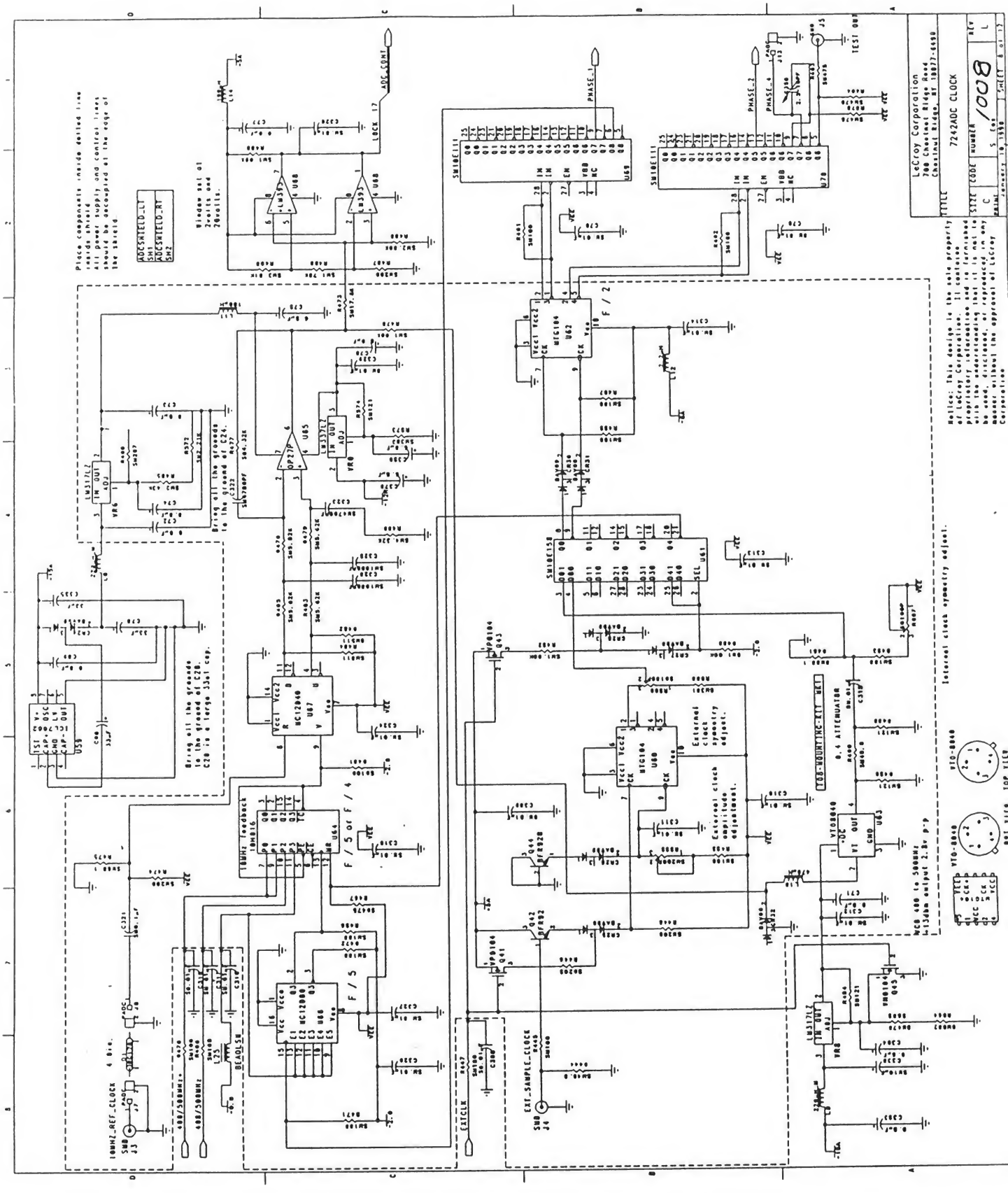


7242ADC **Sheet 5.**

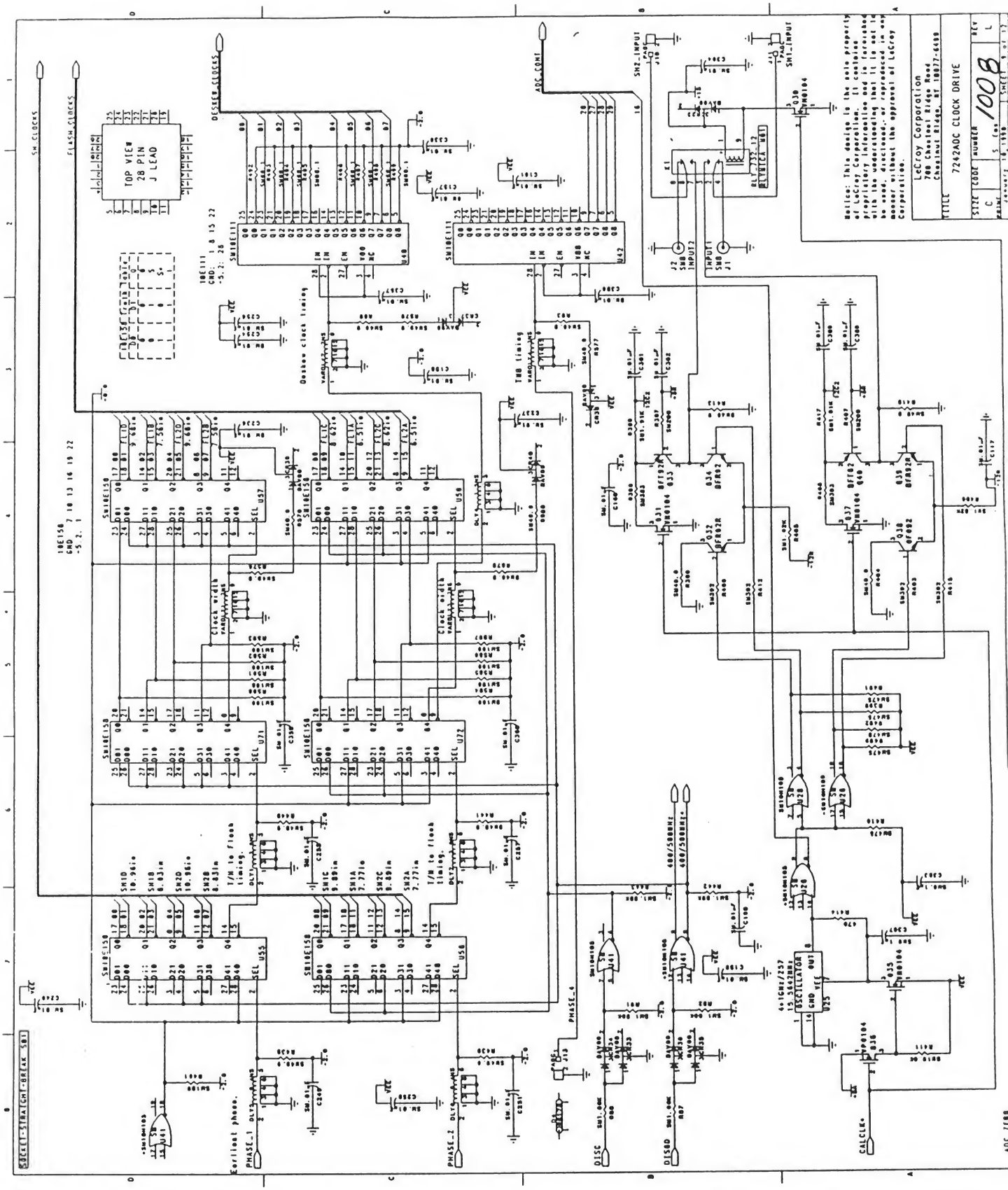

H7242FLASH C
CXA1176K
H7242FLASH A
CXA1176K
H7242FLASH D
CXA1176K
H7242FLASH B
CXA1176K
FL2C
FL2A
FL2D
FL2B
LeCroy Corporation
700 Chestnut Ridge Road
Chestnut Ridge, NY 10977-6499
7242ADC CHANNEL 2 FLASH
1008
ANALOG BUS
FLASH CLOCKS



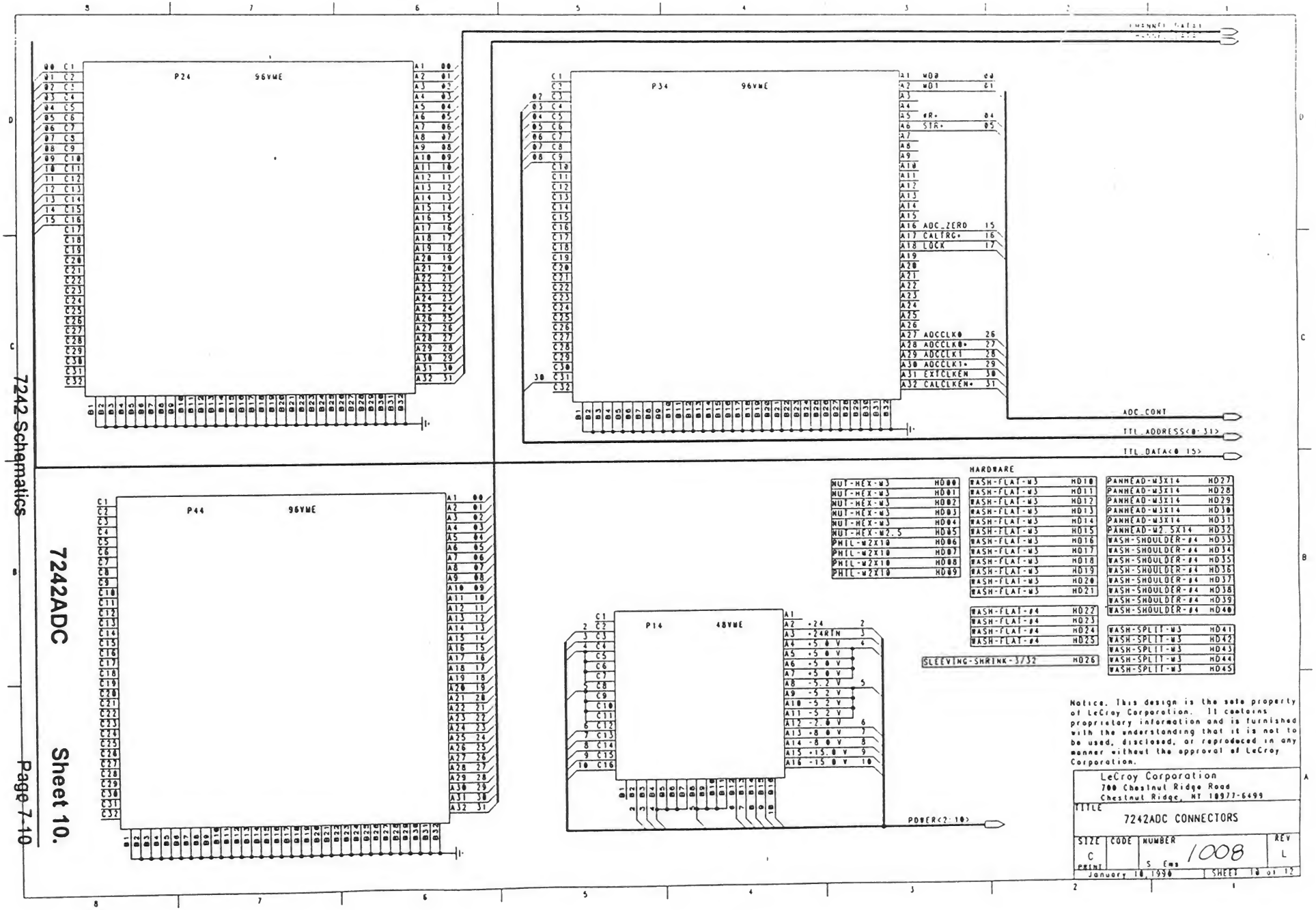
7242ADC **Sheet 7.**



7242ADC **Sheet 8.**



7242ADC **Sheet 9.**



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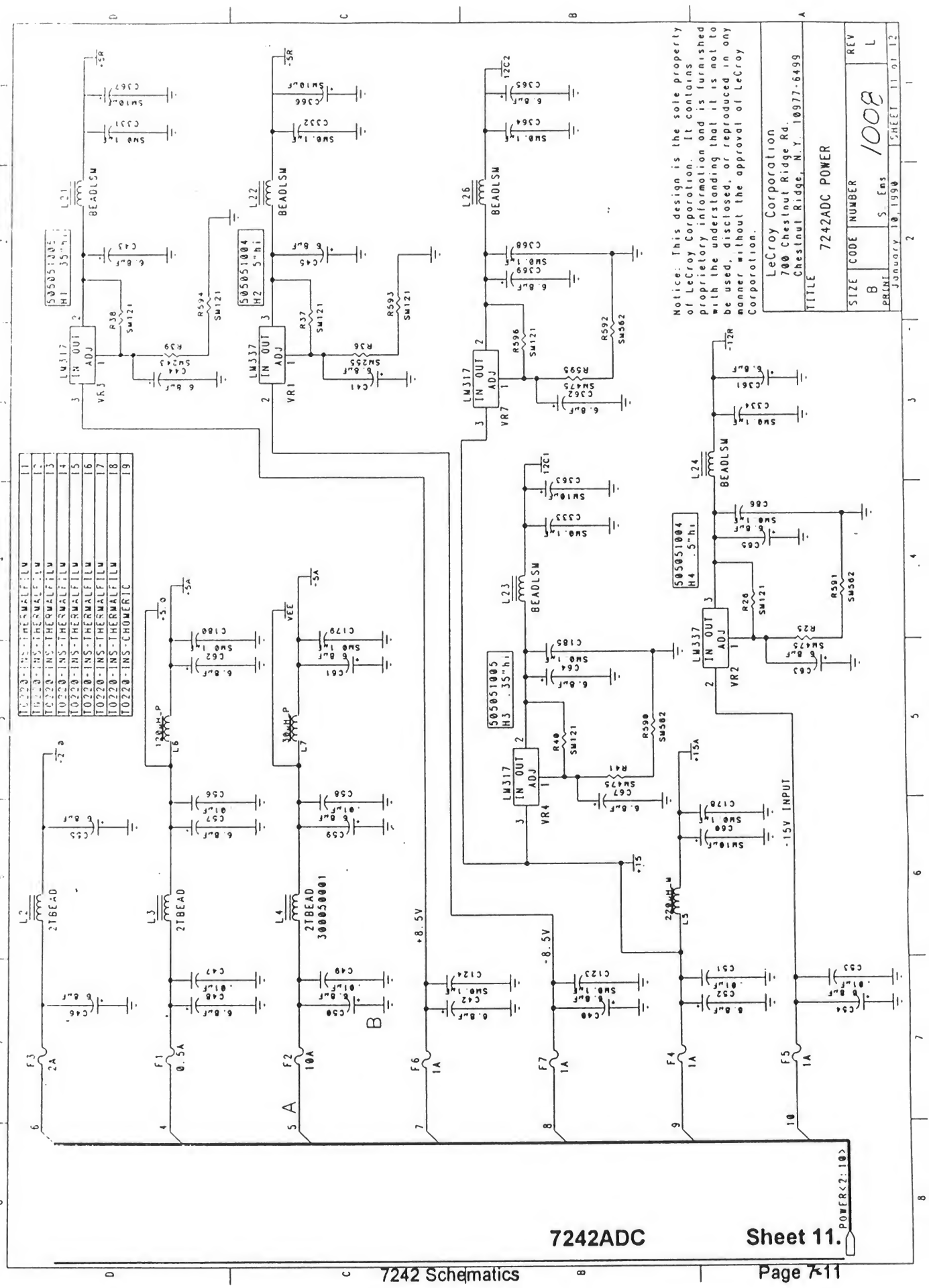
700 Chestnut Ridge Road
Chestnut Ridge, NY 10977-6499

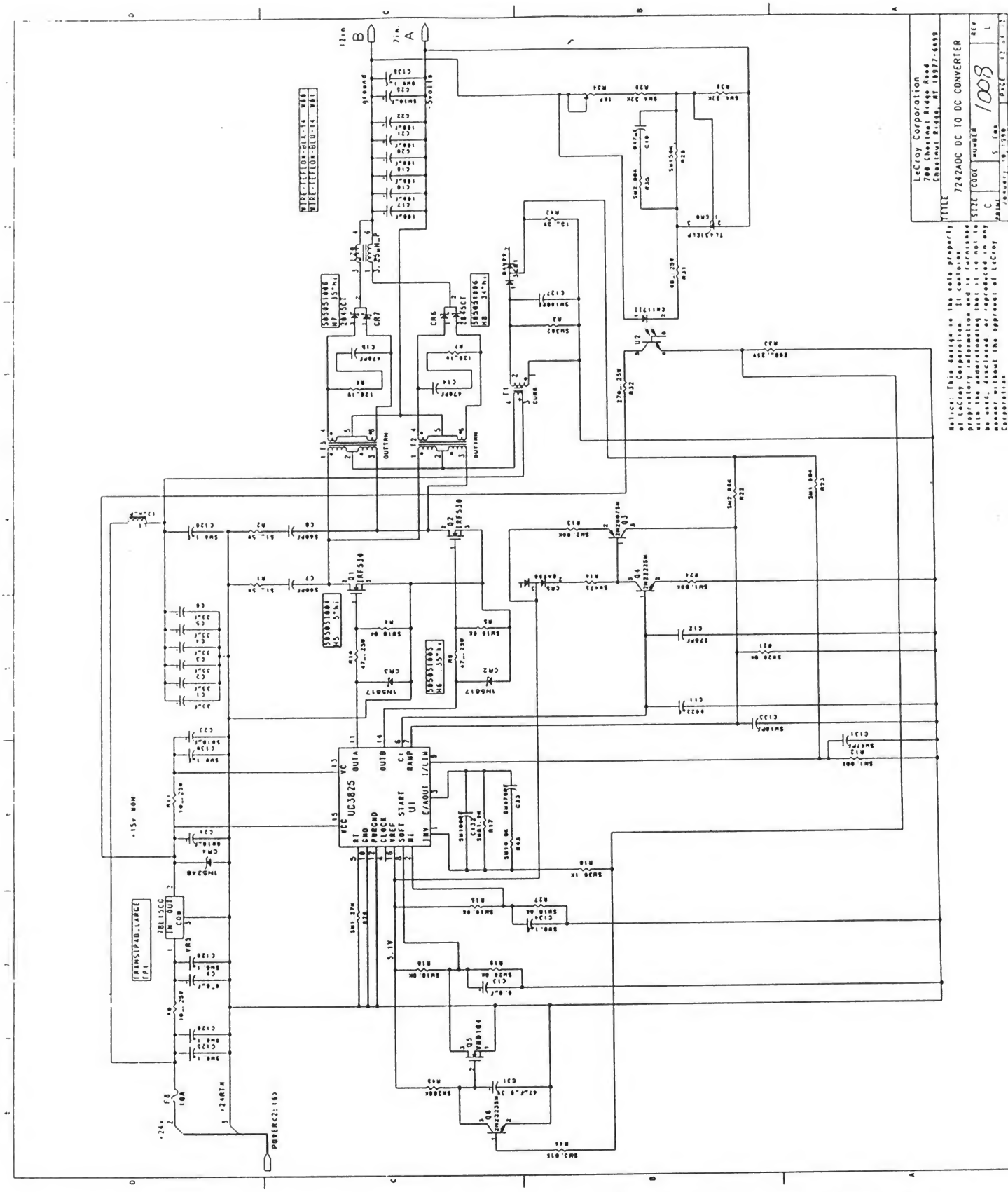
TITLE: 7242ADC CONNECTORS

SIZE	CODE	NUMBER	REV
C		1008	L

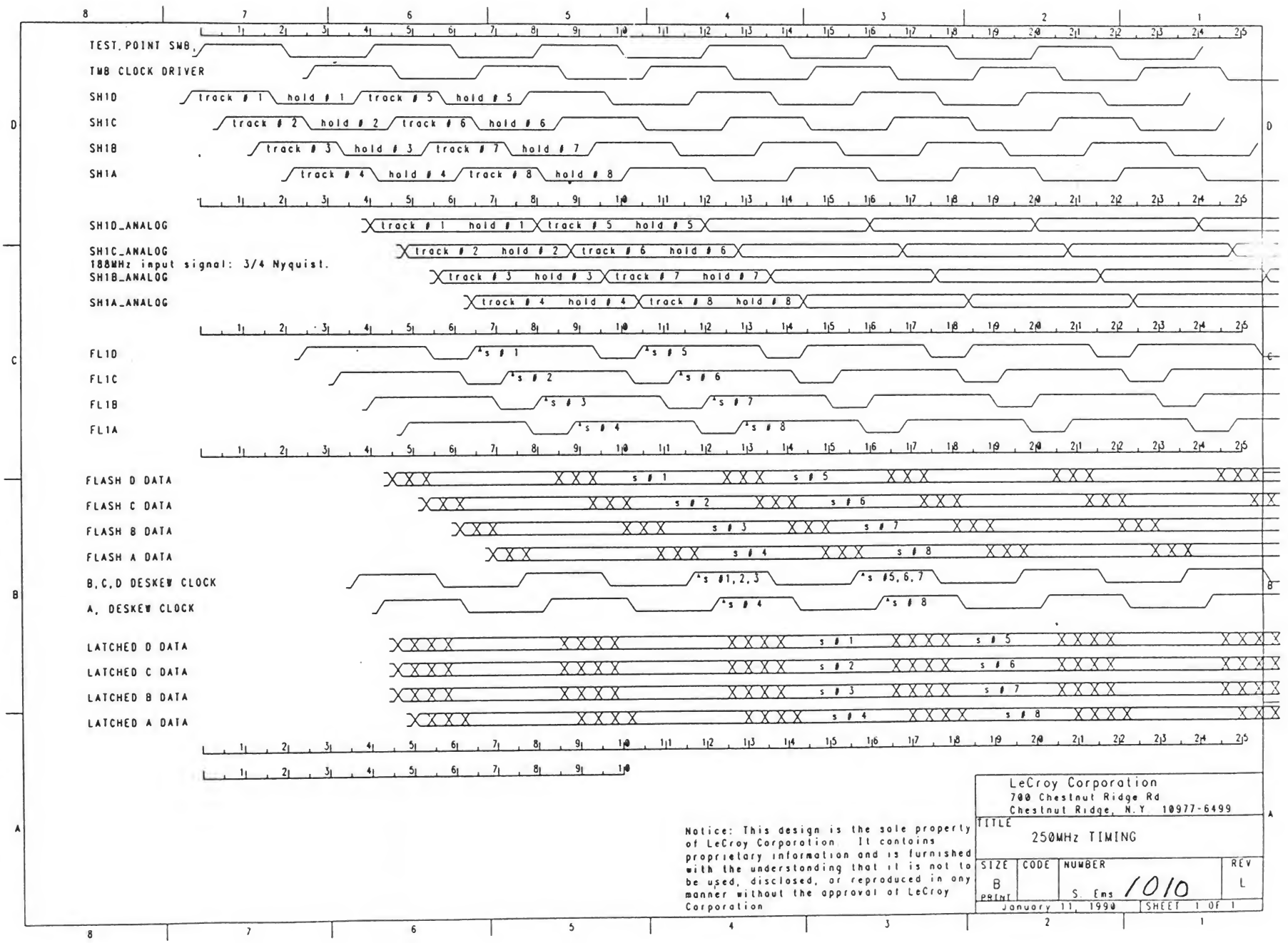
PRINT: S Eng | January 18, 1996 | SHEET 10 of 12

7242ADC Sheet 10.


7242ADC
Sheet 11.



7242ADC **Sheet 12.**


TEST. POINT SMB
TMB CLOCK DRIVER
SH1D
SH1C
SH1B
SH1A
track # 1 hold # 1 track # 5 hold # 5
track # 2 hold # 2 track # 6 hold # 6
track # 3 hold # 3 track # 7 hold # 7
track # 4 hold # 4 track # 8 hold # 8
SH1D_ANALOG
SH1C_ANALOG
188MHz input signal: 3/4 Nyquist.
SH1B_ANALOG
SH1A_ANALOG
FL1D
FL1C
FL1B
FL1A
*s # 1
*s # 5
*s # 2
*s # 6
*s # 3
*s # 7
*s # 4
*s # 8
FLASH D DATA
FLASH C DATA
FLASH B DATA
FLASH A DATA
s # 1
s # 5
s # 2
s # 6
s # 3
s # 7
s # 4
s # 8
B,C,D DESKEW CLOCK
A, DESKEW CLOCK
*s #1, 2, 3
*s #5, 6, 7
LATCHED D DATA
LATCHED C DATA
LATCHED B DATA
LATCHED A DATA
LeCroy Corporation
700 Chestnut Ridge Rd
Chestnut Ridge, N.Y. 10977-6499
TITLE
250MHz TIMING
SIZE B
CODE
NUMBER S. Ems 1010
REV L
January 11, 1990
SHEET 1 OF 1
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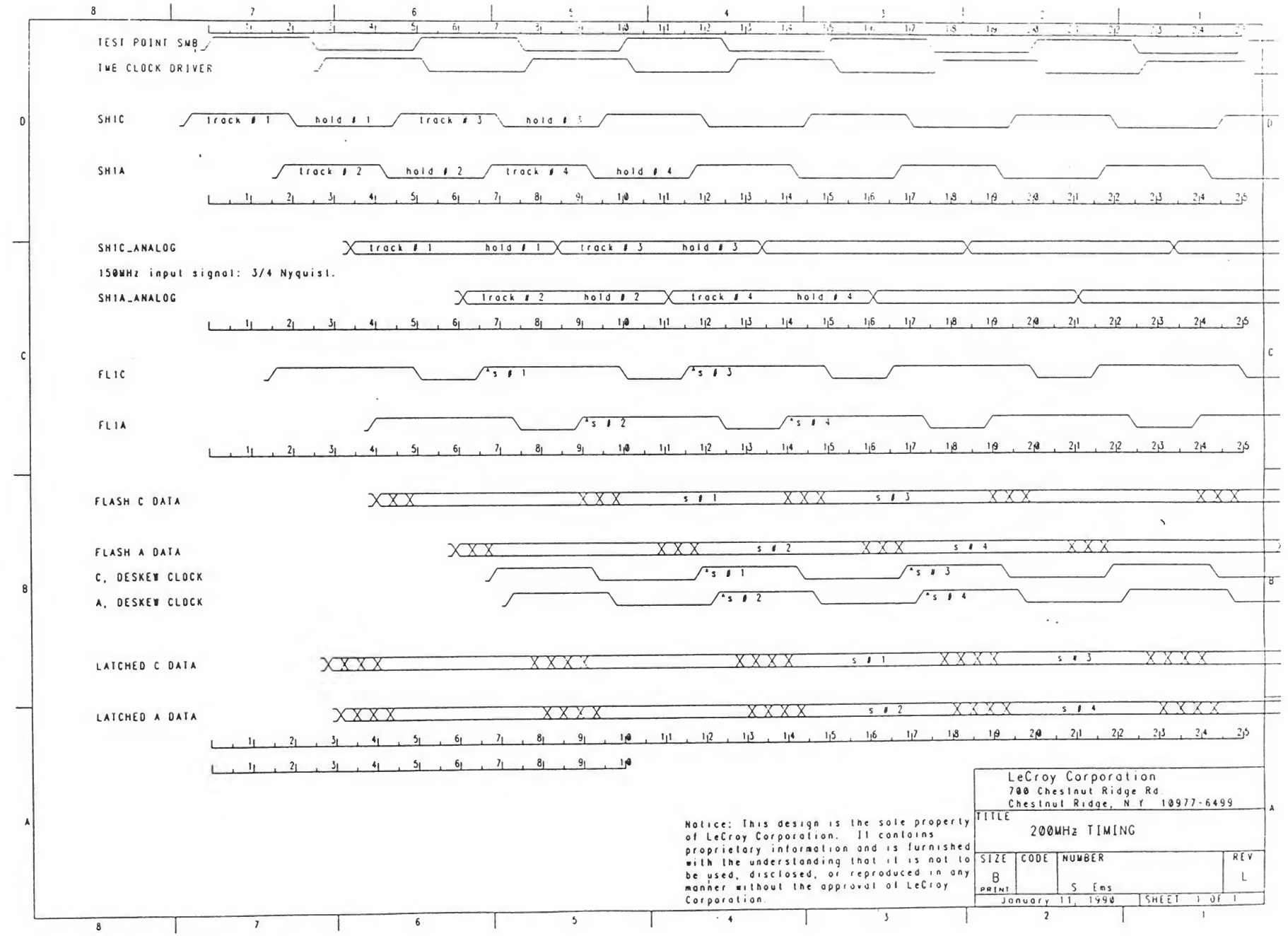
TEST POINT SW8
TWE CLOCK DRIVER
SH1C
track # 1
hold # 1
track # 3
hold # 3
SH1A
track # 2
hold # 2
track # 4
hold # 4
SH1C_ANALOG
SH1A_ANALOG
150MHz input signal: 3/4 Nyquist.
FL1C
FL1A
FLASH C DATA
FLASH A DATA
C, DESKEW CLOCK
A, DESKEW CLOCK
LATCHED C DATA
LATCHED A DATA
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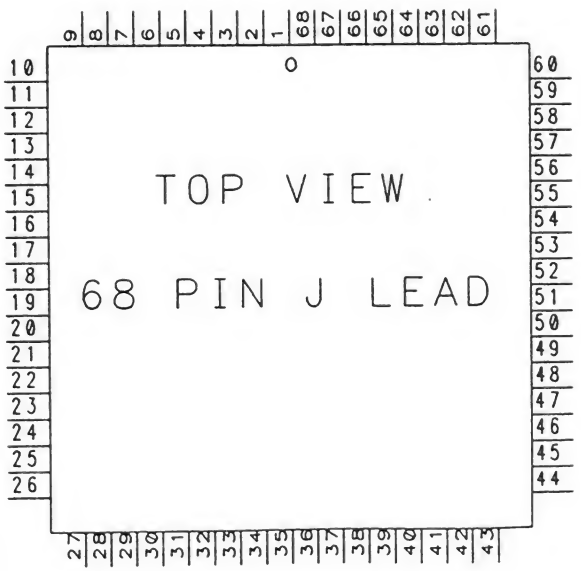
LeCroy Corporation
700 Chestnut Ridge Rd
Chestnut Ridge, N Y 10977-6499
TITLE
200MHz TIMING
SIZE
B
PRINT
CODE
NUMBER
S Ems
REV
L
January 11, 1990
SHEET 1 OF 1

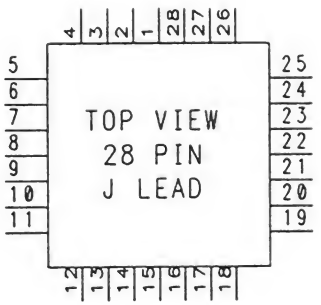
2	DAC
3	SH1
4	FLASH1
5	SH2
6	FLASH2
7	DATA
8	CLOCK
9	CLKDRIVE
10	CONNECT
11	POWER
12	DCDC
13	ECONOTES
14	HARDWARE
	TIME4NS

TIMING
LAYOUT
PARTS

7242ADC MEMORY MAP

ADDRESS	LOWER BYTE FUNCTION	UPPER BYTE FUNCTION
40000000	CH1 FLASH A GAIN	CH1 COARSE S_H A OFFSET
40000004	CH1 FLASH B GAIN	CH1 FINE S_H A OFFSET
40000008	CH1 FLASH C GAIN	CH1 COARSE S_H B OFFSET
4000000C	CH1 FLASH D GAIN	CH1 FINE S_H B OFFSET
40000010	CH1 S_H A DELAY	CH1 COARSE S_H C OFFSET
40000014	CH1 S_H B DELAY	CH1 FINE S_H C OFFSET
40000018	CH1 S_H C DELAY	CH1 COARSE S_H D OFFSET
4000001C	CH1 S_H D DELAY	CH1 FINE S_H D OFFSET
40000020	CH2 FLASH A GAIN	CH2 COARSE S_H A OFFSET
40000024	CH2 FLASH B GAIN	CH2 FINE S_H A OFFSET
40000028	CH2 FLASH C GAIN	CH2 COARSE S_H B OFFSET
4000002C	CH2 FLASH D GAIN	CH2 FINE S_H B OFFSET
40000030	CH2 S_H A DELAY	CH2 COARSE S_H C OFFSET
40000034	CH2 S_H B DELAY	CH2 FINE S_H C OFFSET
40000038	CH2 S_H C DELAY	CH2 COARSE S_H D OFFSET
4000003C	CH2 S_H D DELAY	CH2 FINE S_H D OFFSET



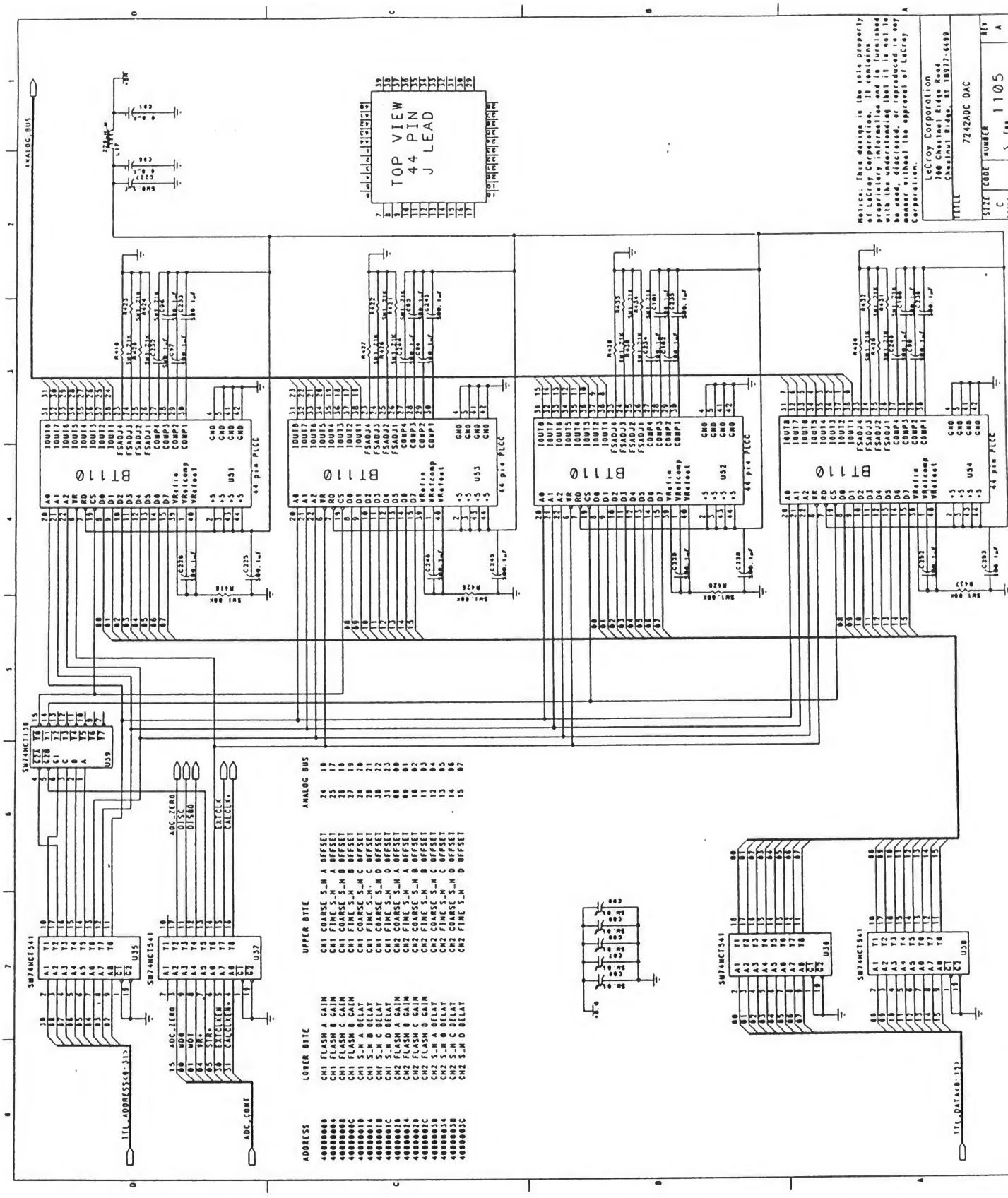


LeCroy Corporation
700 Chestnut Ridge Road.
Chestnut Ridge, NY 10977-6499

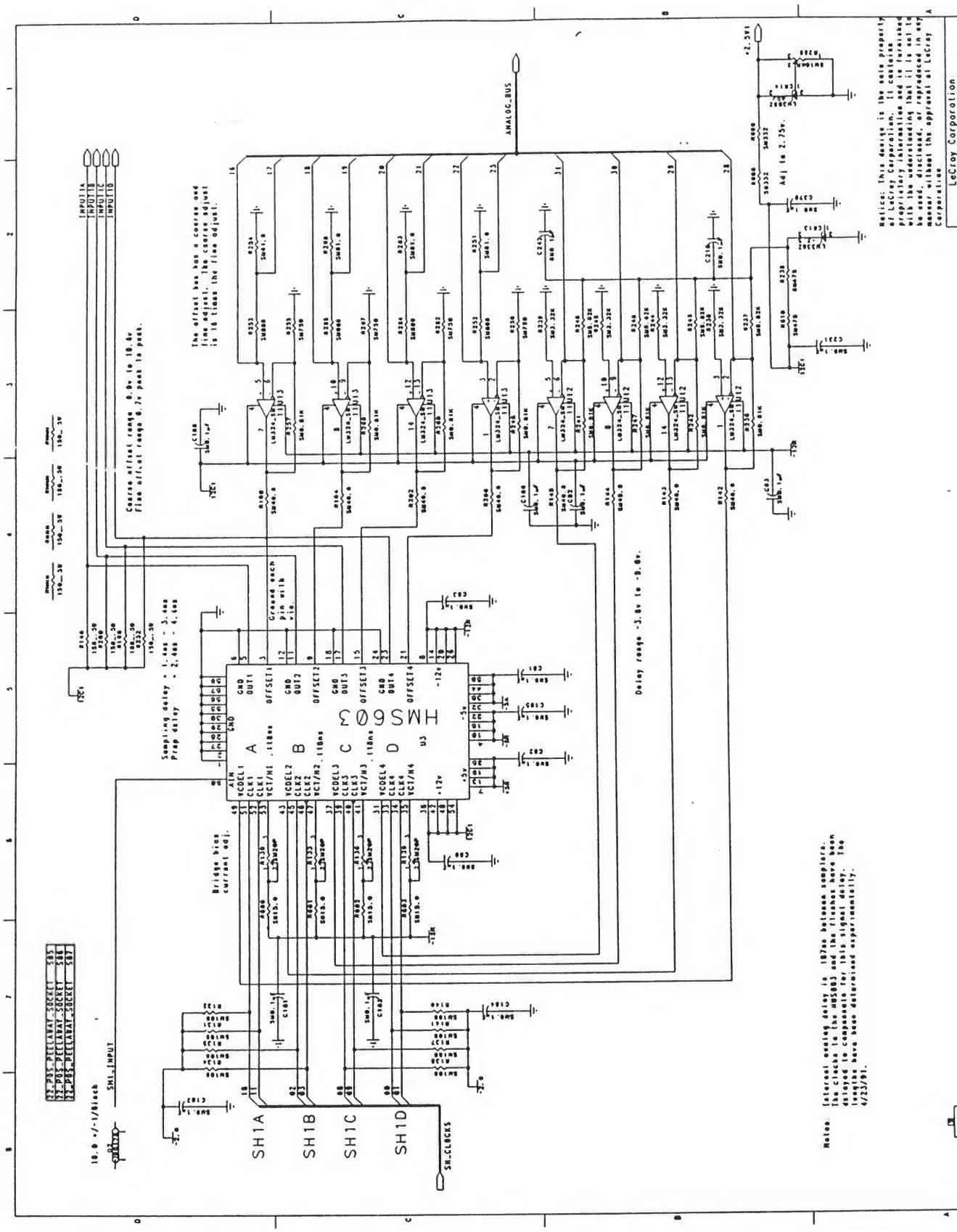
TITLE 7242ADCA

SIZE	CODE	NUMBER	REV
A		1105	A
PRINT		S. Ems	

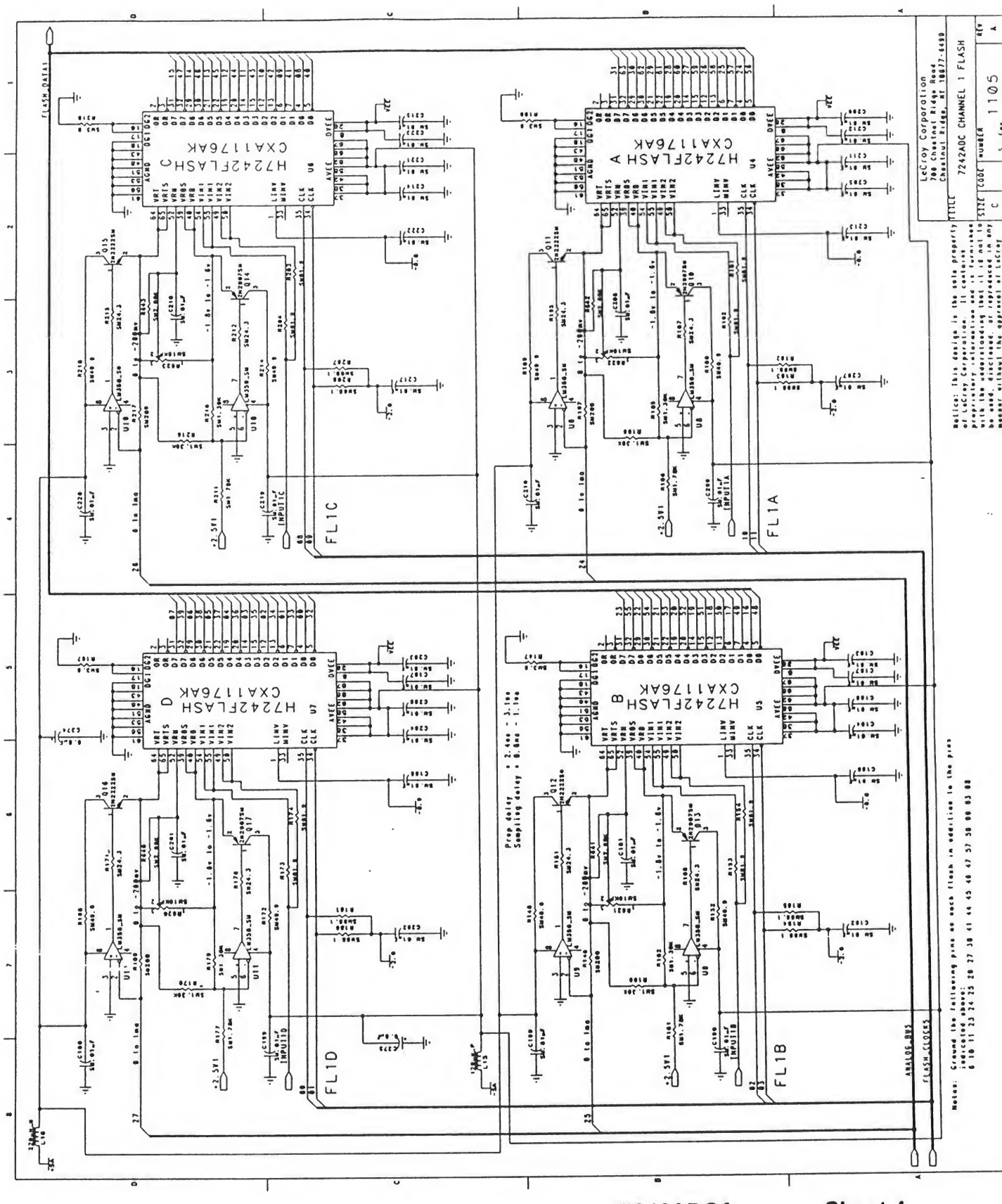
October 8, 1992 SHEET 1 of 14



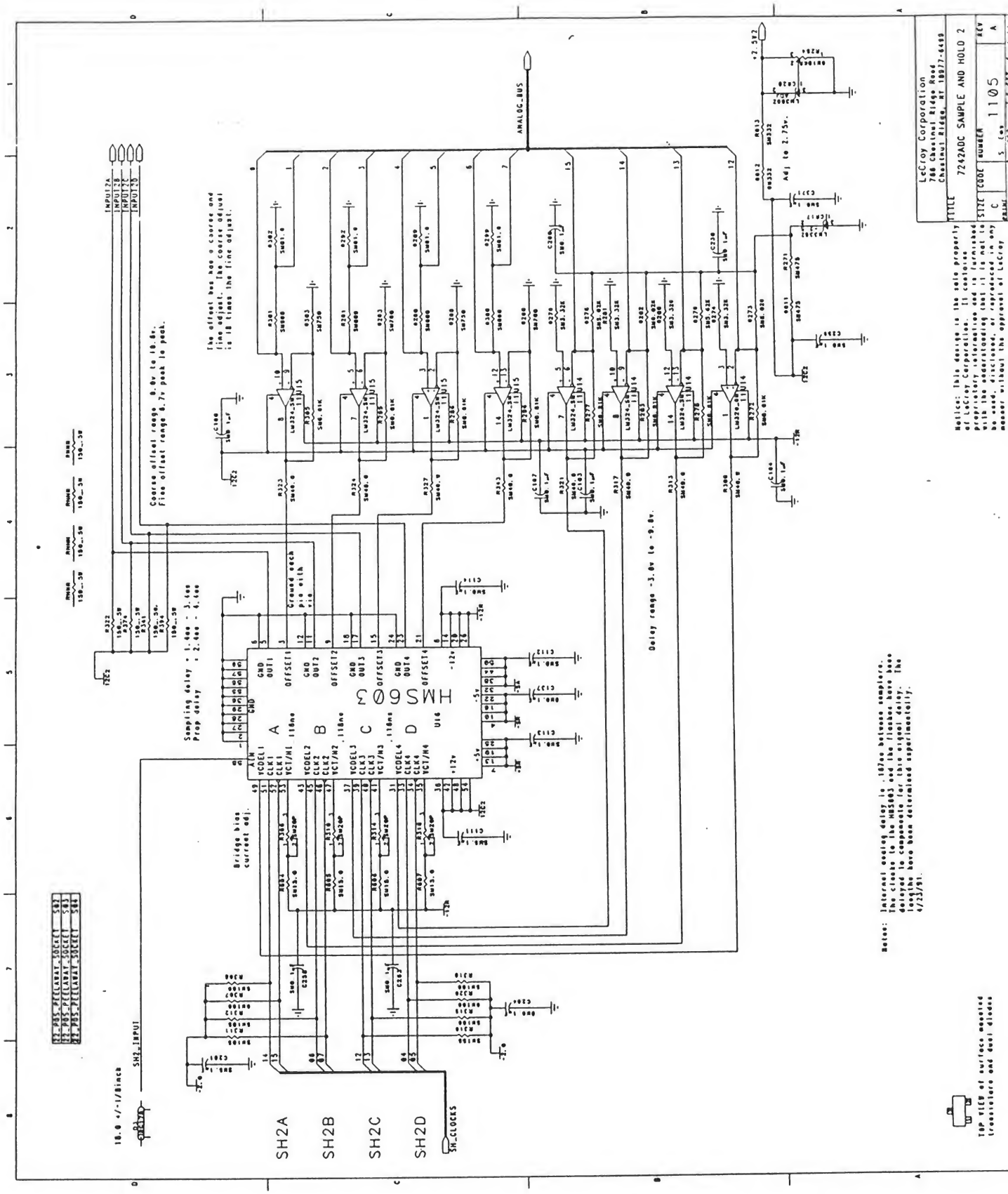
7242ADCA **Sheet 2.**

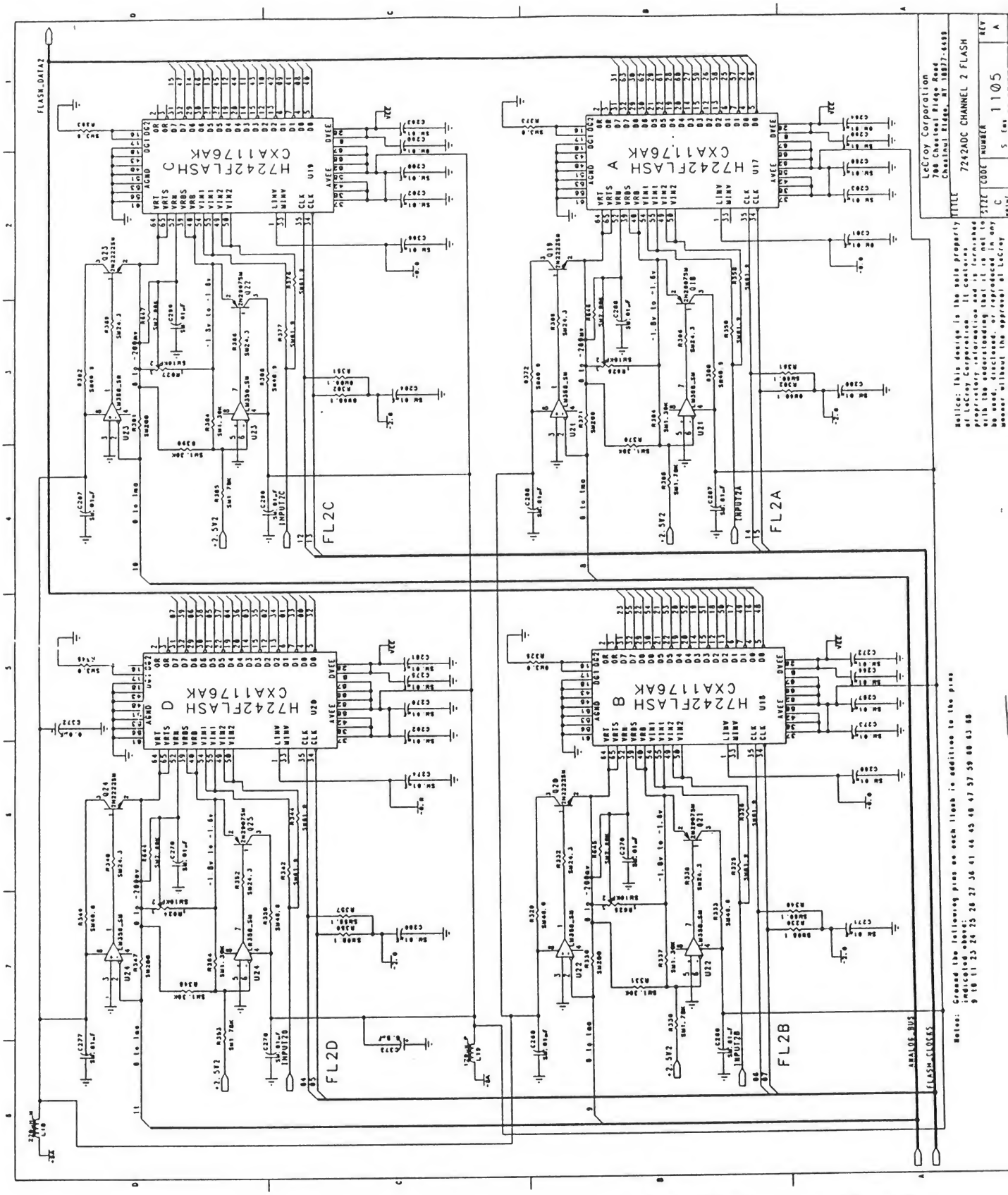


7242ADCA **Sheet 3.**



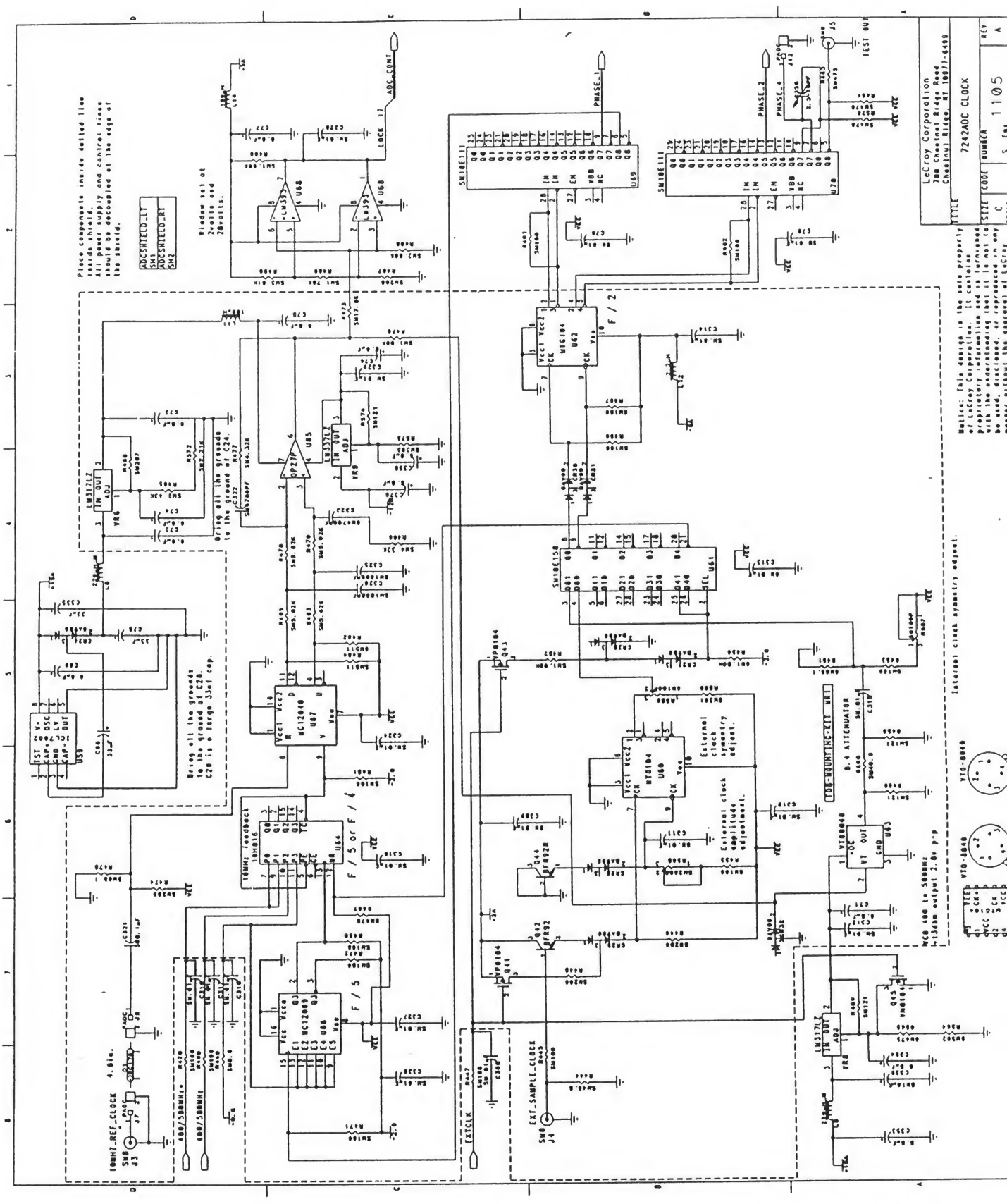
7242ADCA **Sheet 4.**


HMS603
SH2A
SH2B
SH2C
SH2D
SH_CLOCKS
SH2_INPUT
ANALOG_BUS
LeCroy Corporation
7242ADC SAMPLE AND HOLD 2
7242ADCA
Sheet 5.



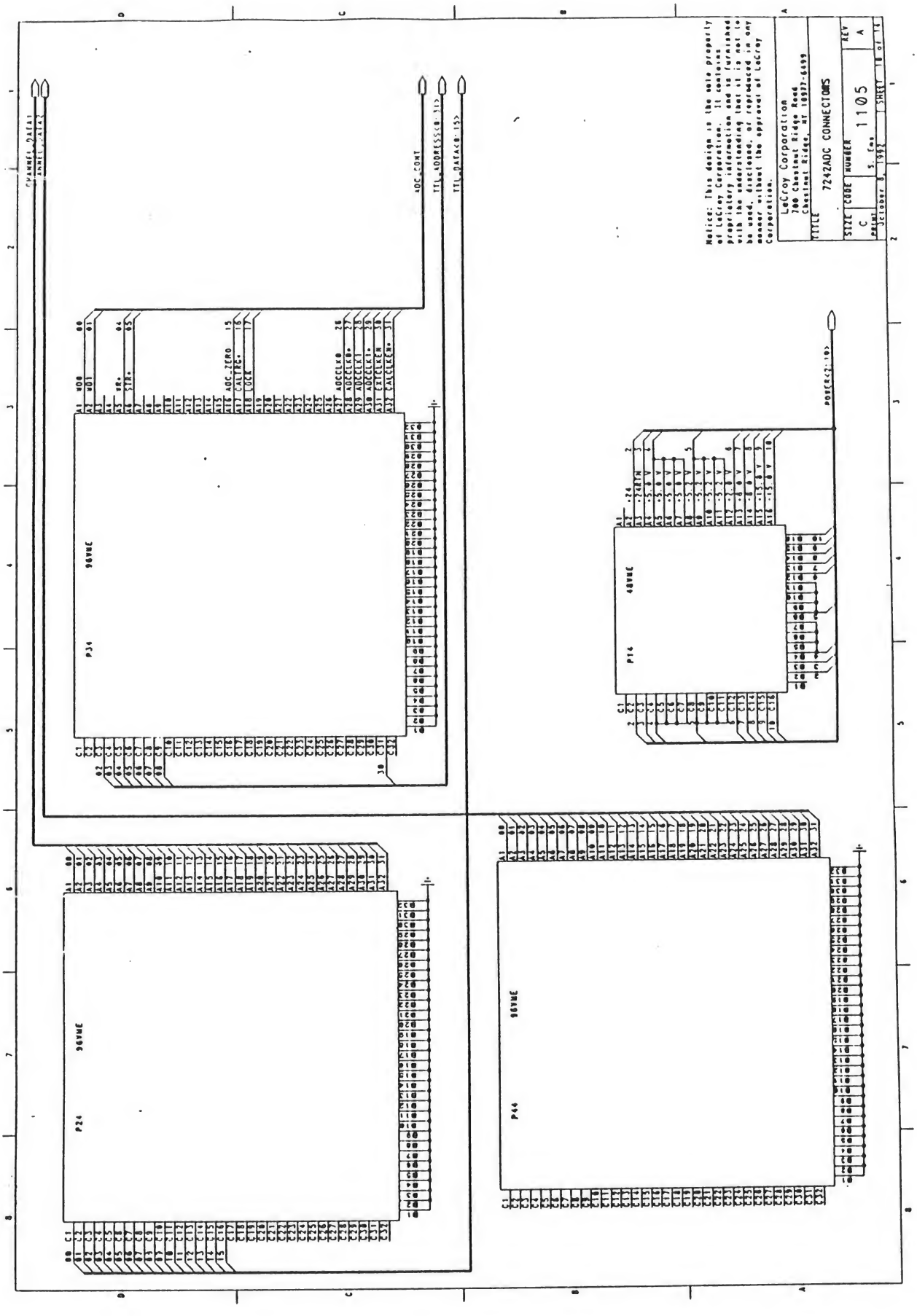
7242ADCA **Sheet 6.**

7242ADCA **Sheet 7.**



7242ADCA **Sheet 8.**

7242ADCA **Sheet 9.**


LeCroy Corporation
700 Chestnut Ridge Road
Chestnut Ridge, NY 10977-6499
TITLE 7242ADC CONNECTORS
SIZE C
CODE
NUMBER 1105
REV A
DATE October 8, 1993
SHEET 10 of 11
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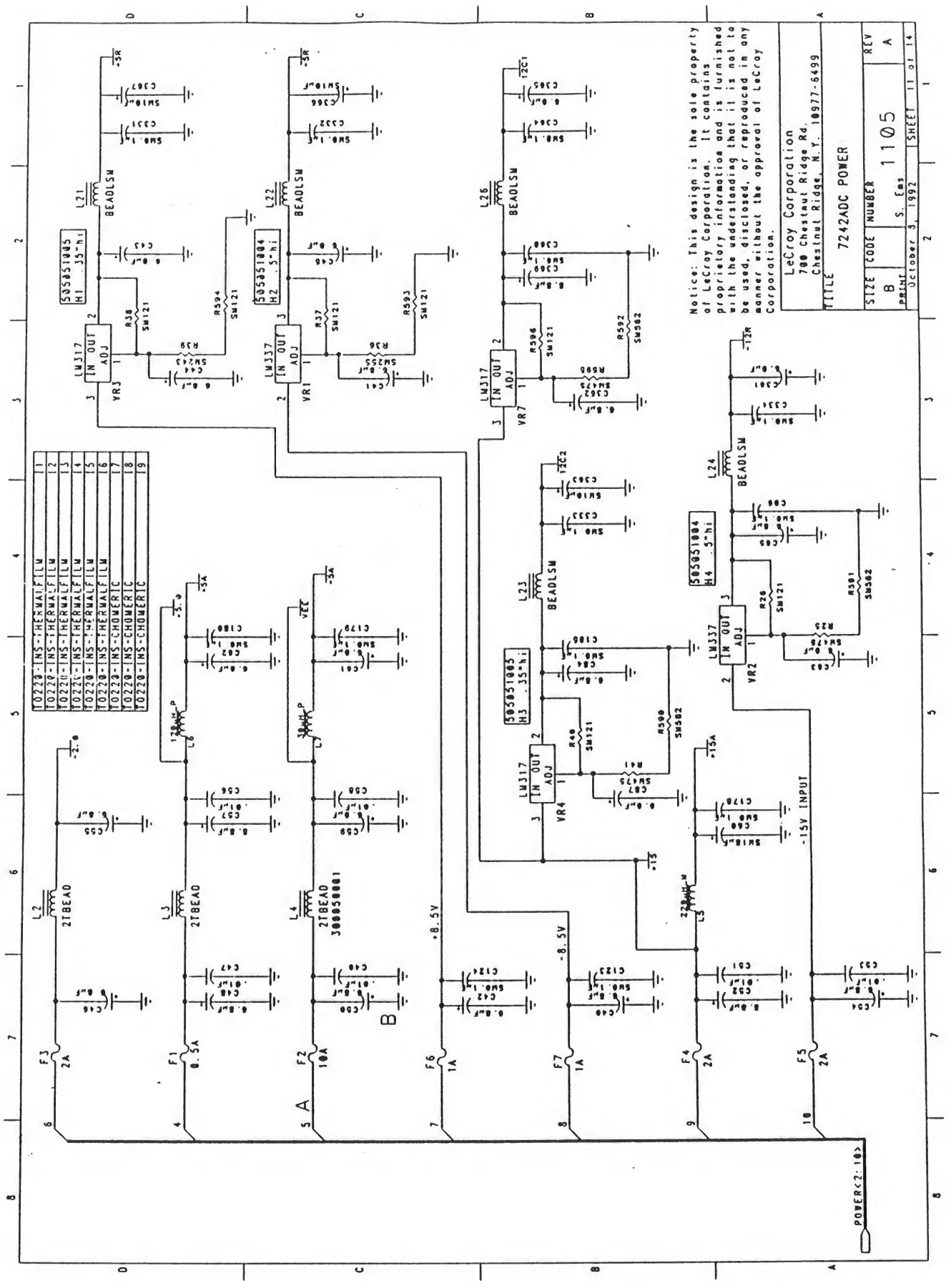
ADC_CONT
TTL_ADDRESS<8:31>
TTL_DATA<0:15>
CHANNEL_DATA<1>
CHANNEL_DATA<2>
P34
96VME
P24
96VME
P14
48VME
P44
96VME


LeCroy Corporation
700 Chestnut Ridge Rd.
Chestnut Ridge, N.Y. 10977-6499
TITLE
7242ADC POWER
SIZE B
CODE
NUMBER 1105
REV A
DRAWN S. Eas
October 3, 1992
SHEET 11 of 14
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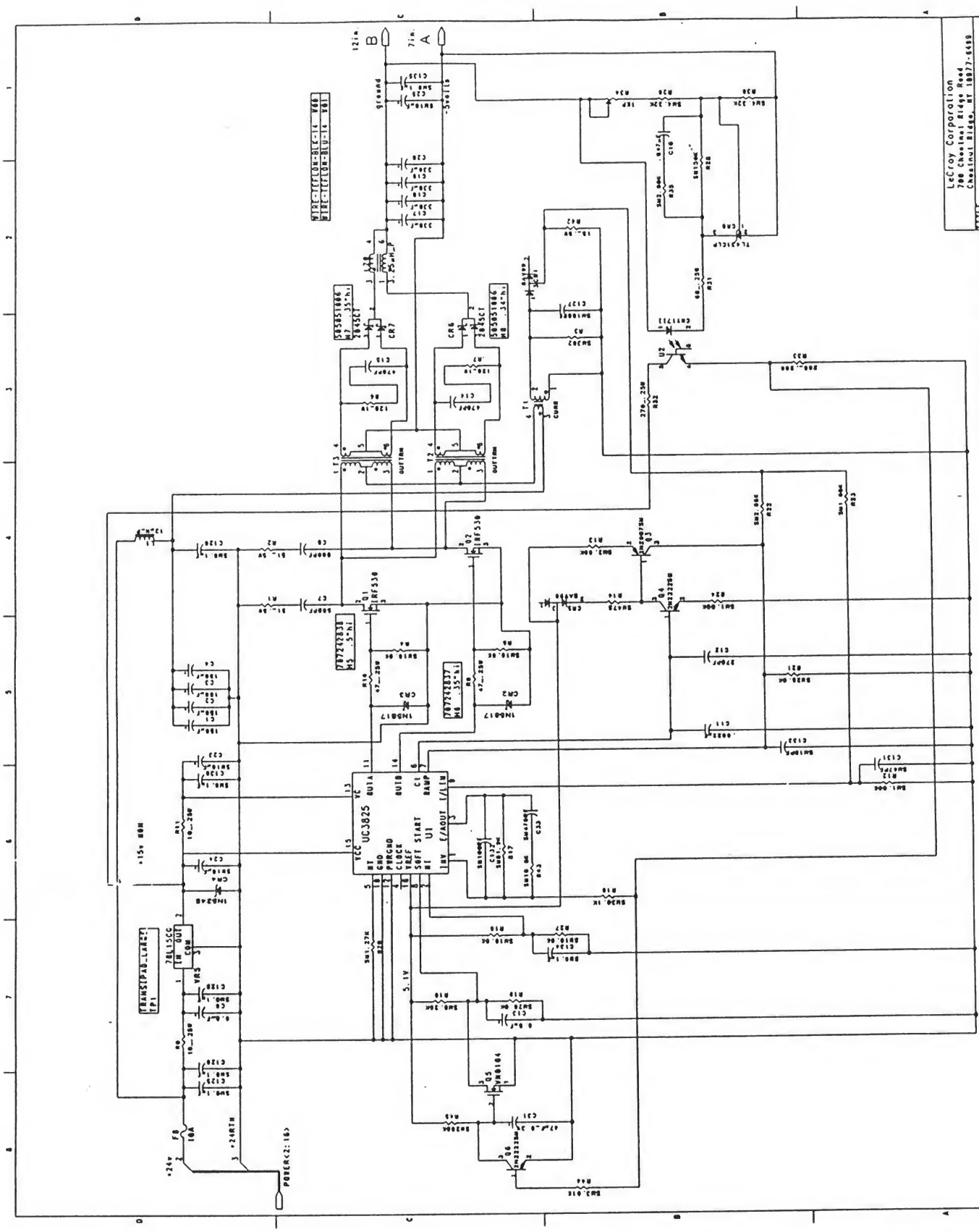
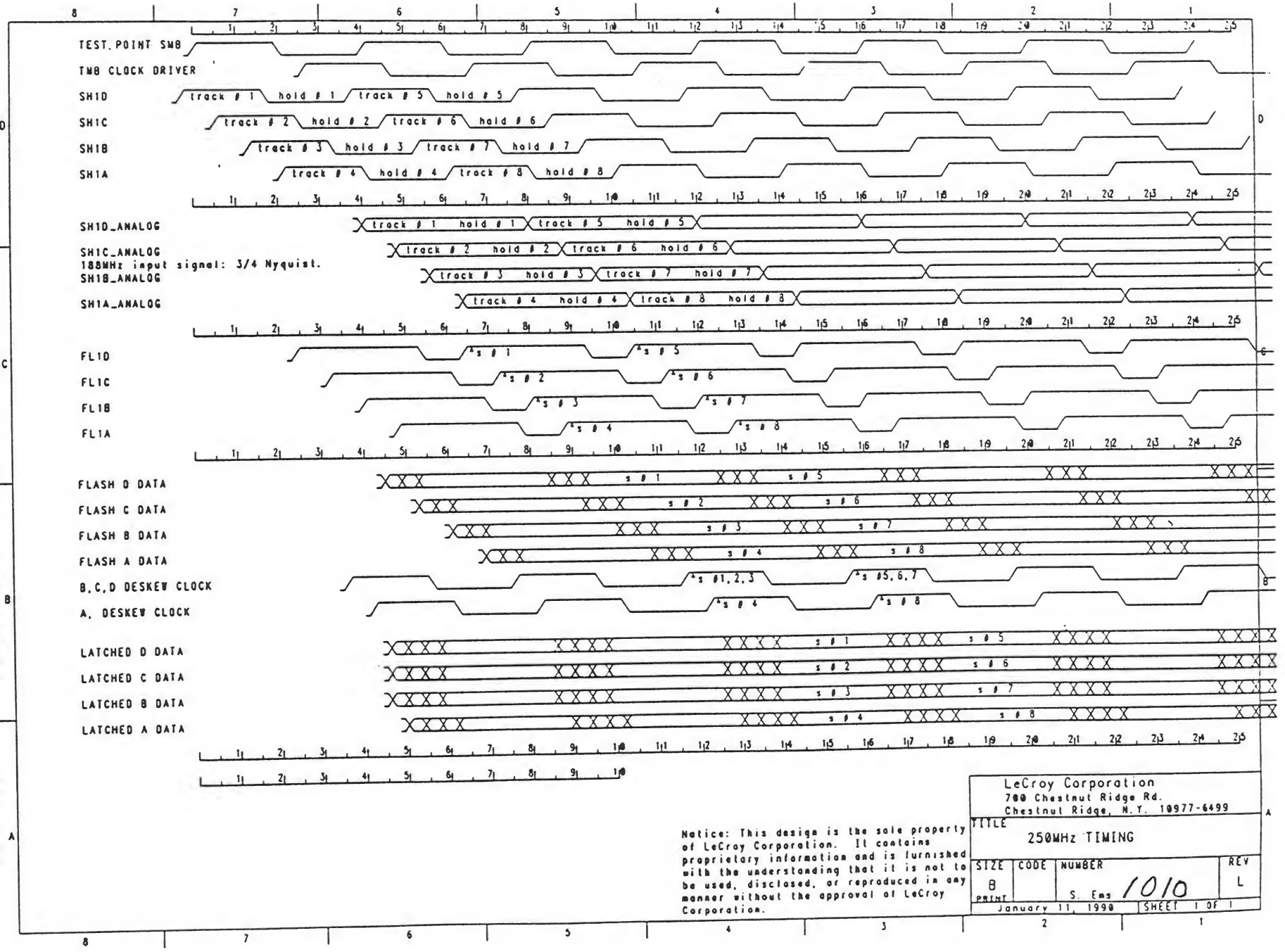
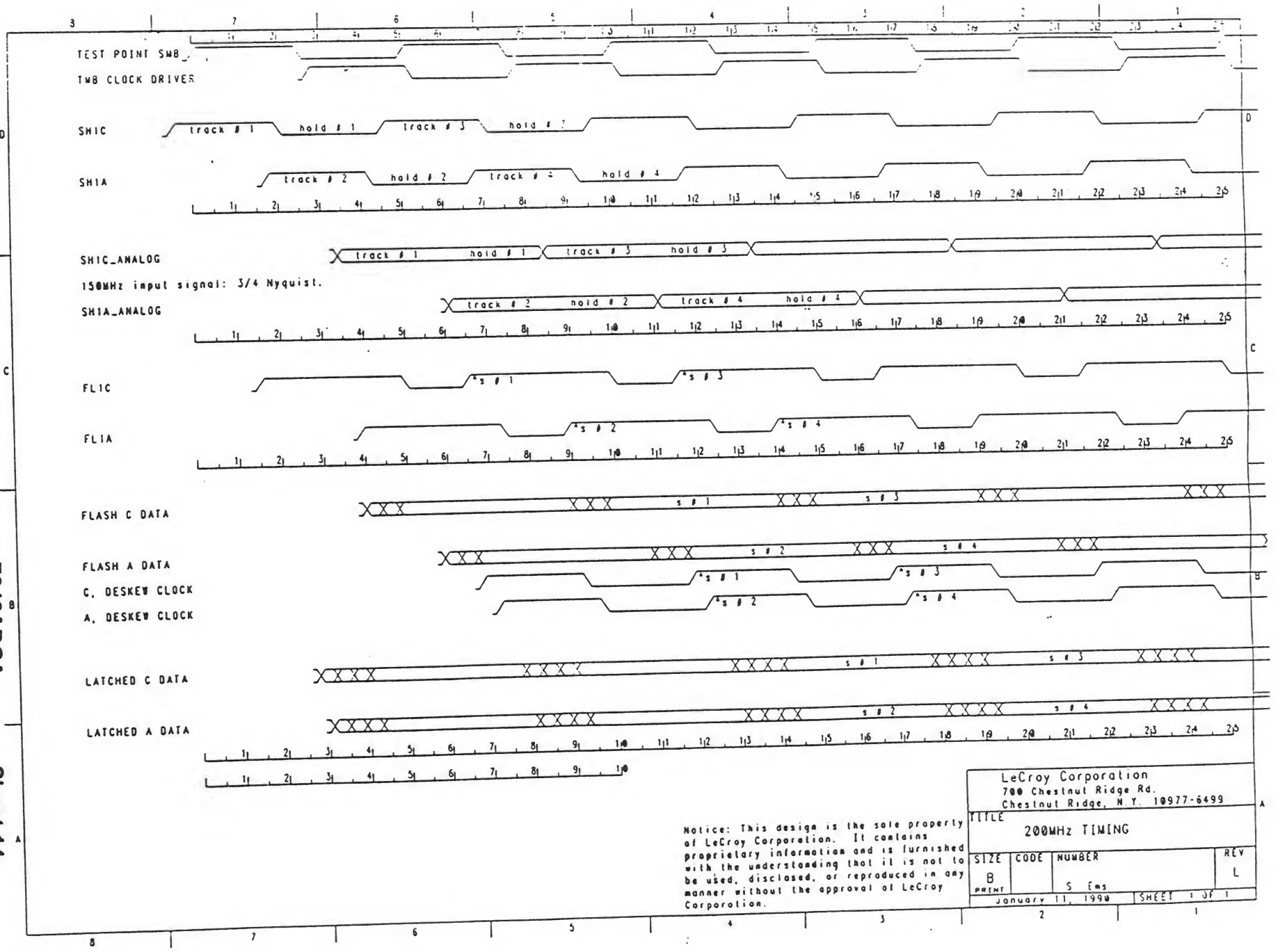
TO220-INS-THERMALFILM
TO220-INS-CHOMERIC
LM317
LM337
BEADLSM
2TBEAD
POWER<2:10>



7242ADCA **Sheet 12.**


TEST. POINT SMB
TMB CLOCK DRIVER
SH1D
SH1C
SH1B
SH1A
track # 1 hold # 1 track # 5 hold # 5
track # 2 hold # 2 track # 6 hold # 6
track # 3 hold # 3 track # 7 hold # 7
track # 4 hold # 4 track # 8 hold # 8
SH1D_ANALOG
SH1C_ANALOG
188MHz input signal: 3/4 Nyquist.
SH1B_ANALOG
SH1A_ANALOG
FL1D
FL1C
FL1B
FL1A
FLASH D DATA
FLASH C DATA
FLASH B DATA
FLASH A DATA
B,C,D DESKEW CLOCK
A, DESKEW CLOCK
LATCHED D DATA
LATCHED C DATA
LATCHED B DATA
LATCHED A DATA
LeCroy Corporation
700 Chestnut Ridge Rd.
Chestnut Ridge, N.Y. 10977-6499
TITLE
250MHz TIMING
SIZE B
CODE
NUMBER S. Ems 1010
REV L
PRINT January 11, 1990
SHEET 1 OF 1
Notice: This design is the sole property of LeCroy Corporation. It contains proprietary information and is furnished with the understanding that it is not to be used, disclosed, or reproduced in any manner without the approval of LeCroy Corporation.


TEST POINT SW8
SW8 CLOCK DRIVES
SH1C
track # 1
hold # 1
track # 3
hold # 3
SH1A
track # 2
hold # 2
track # 4
hold # 4
SH1C_ANALOG
SH1A_ANALOG
150MHz input signal: 3/4 Nyquist.
FL1C
FL1A
FLASH C DATA
FLASH A DATA
C. DESKEW CLOCK
A. DESKEW CLOCK
LATCHED C DATA
LATCHED A DATA
LeCroy Corporation
700 Chestnut Ridge Rd.
Chestnut Ridge, N.Y. 10977-6499
TITLE
200MHz TIMING
SIZE
B
PRINT
CODE
NUMBER
S Ems
REV
L
January 11, 1990
SHEET 1 OF 1
Notice: This design is the sole property of LeCroy Corporation. It contains proprietary information and is furnished with the understanding that it is not to be used, disclosed, or reproduced in any manner without the approval of LeCroy Corporation.

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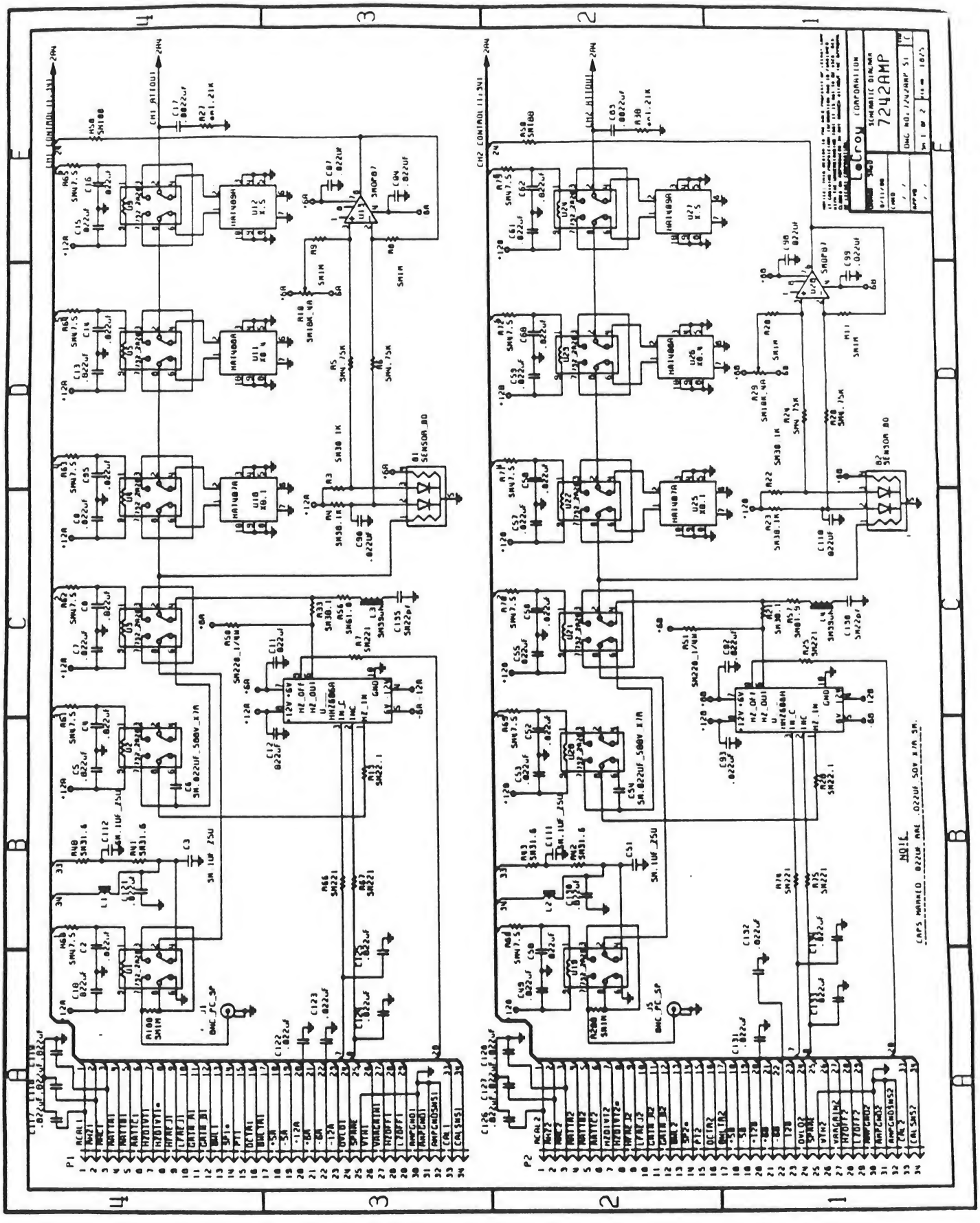
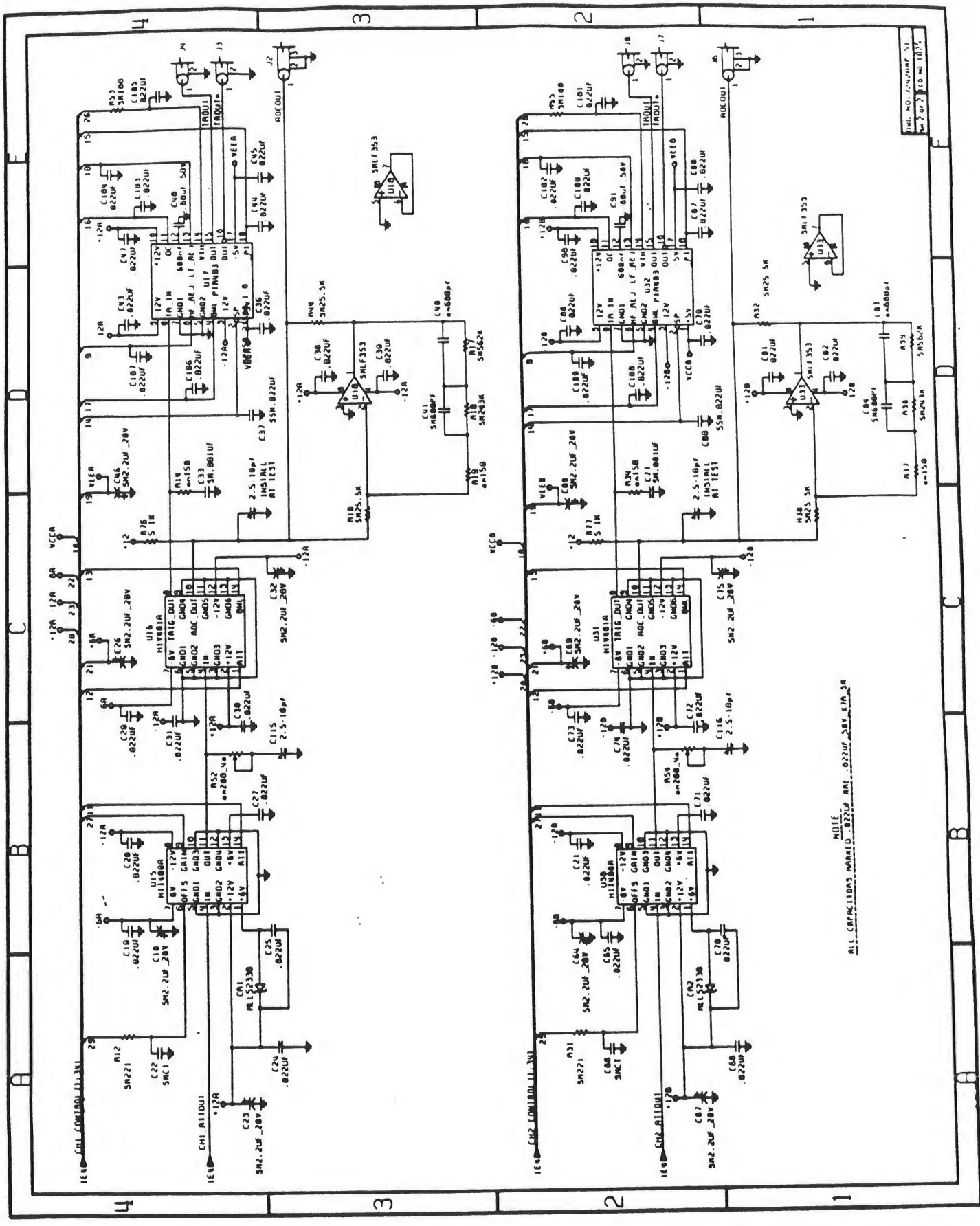
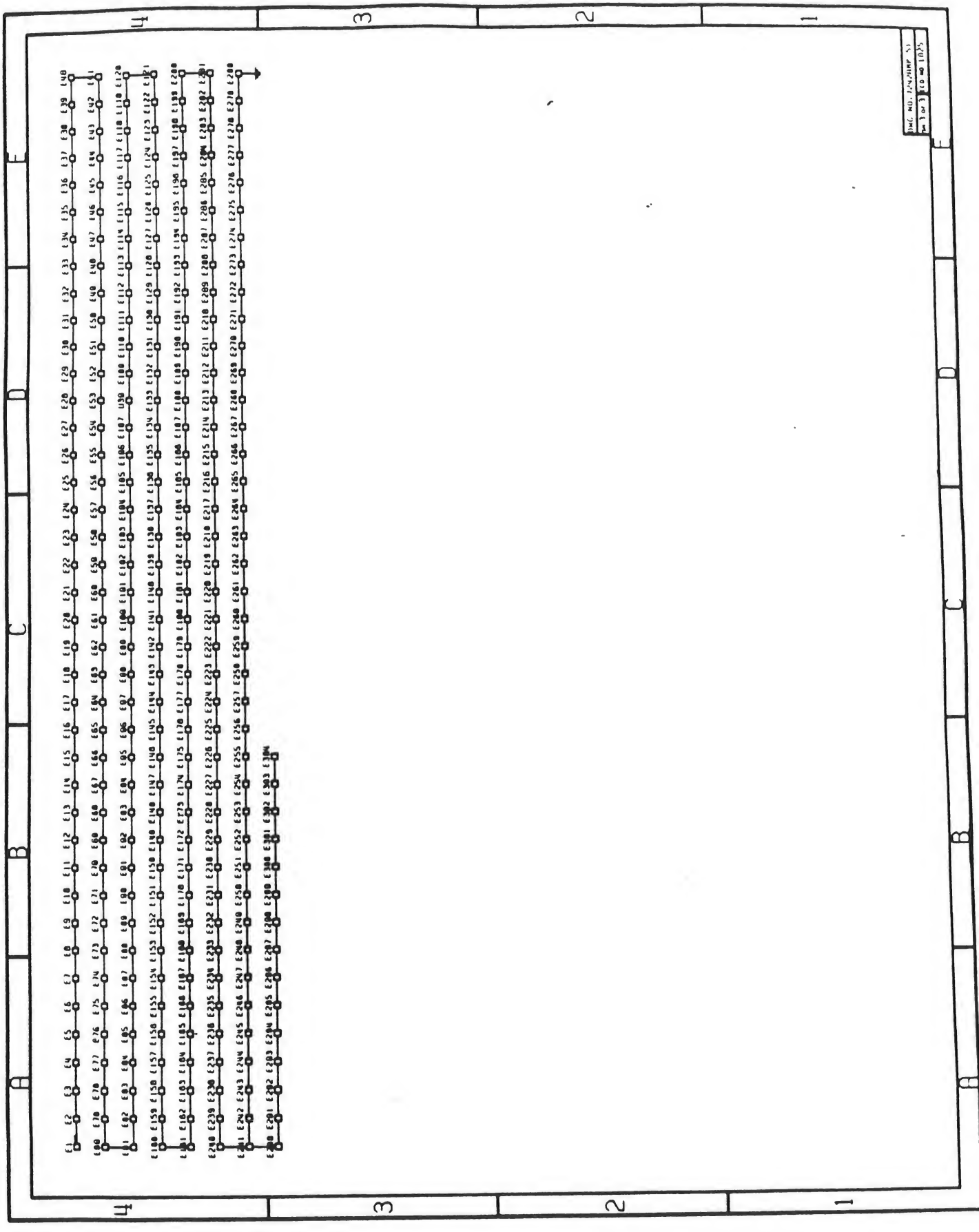


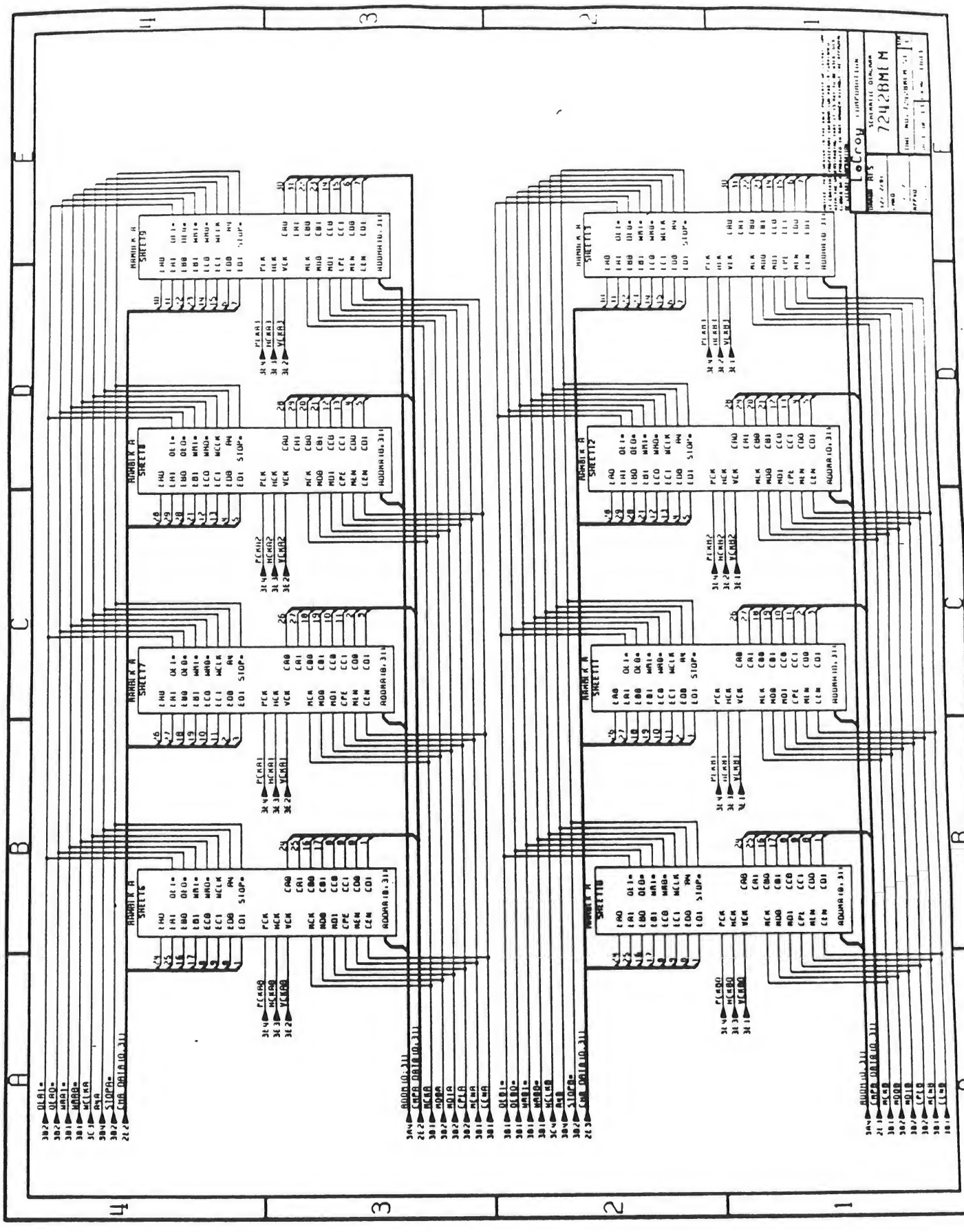
7242AMP **Sheet 1.**

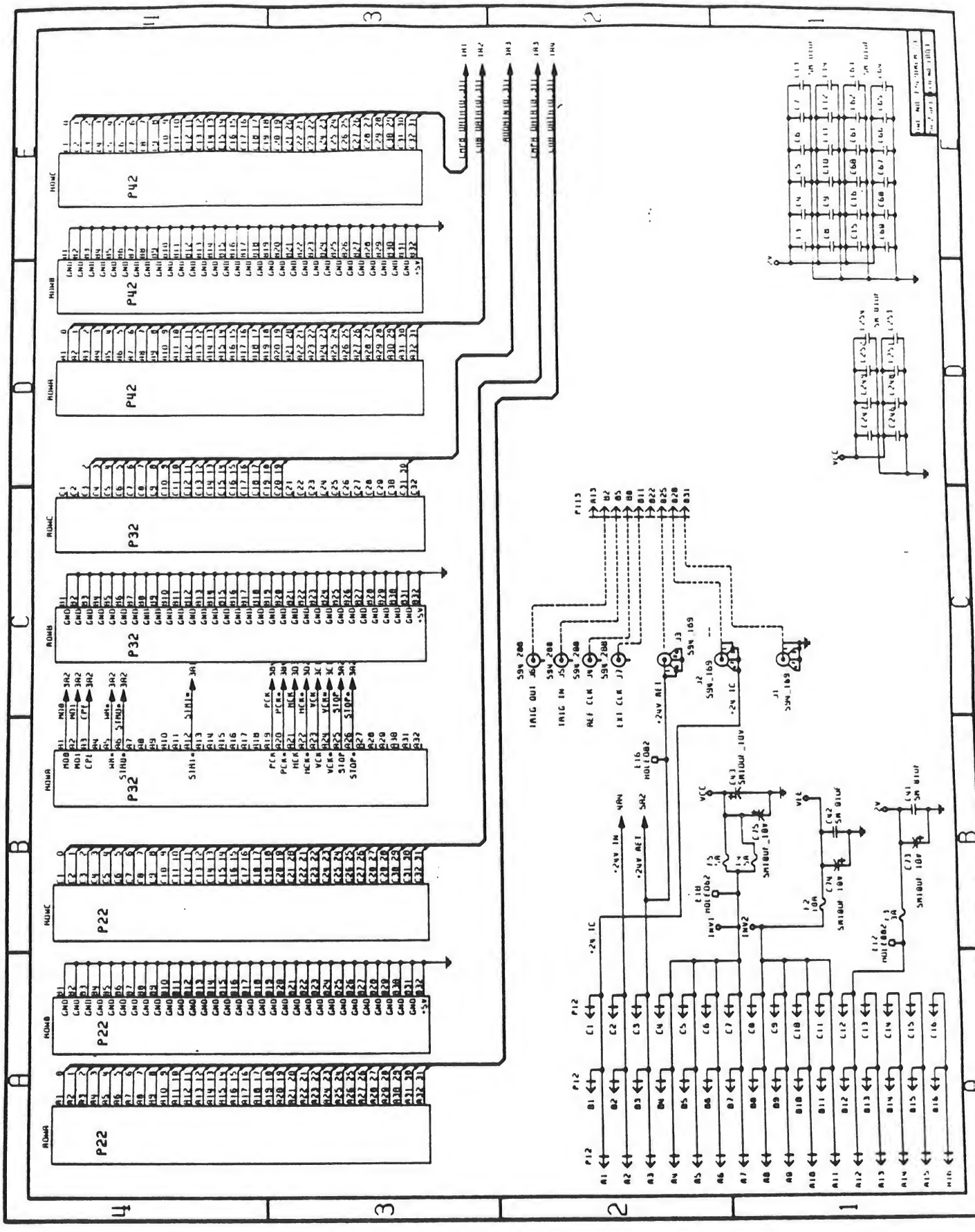


7242AMP **Sheet 2.**

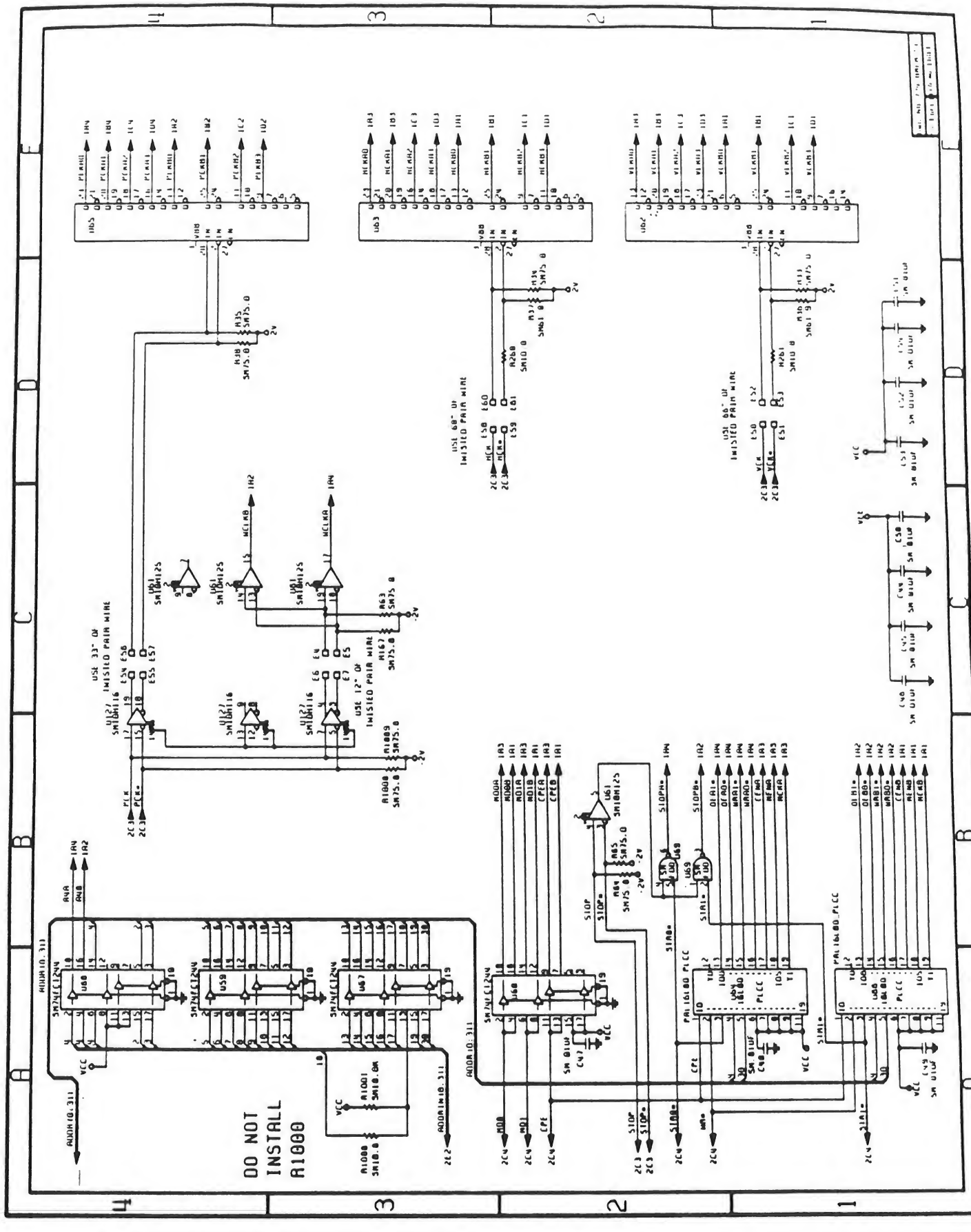


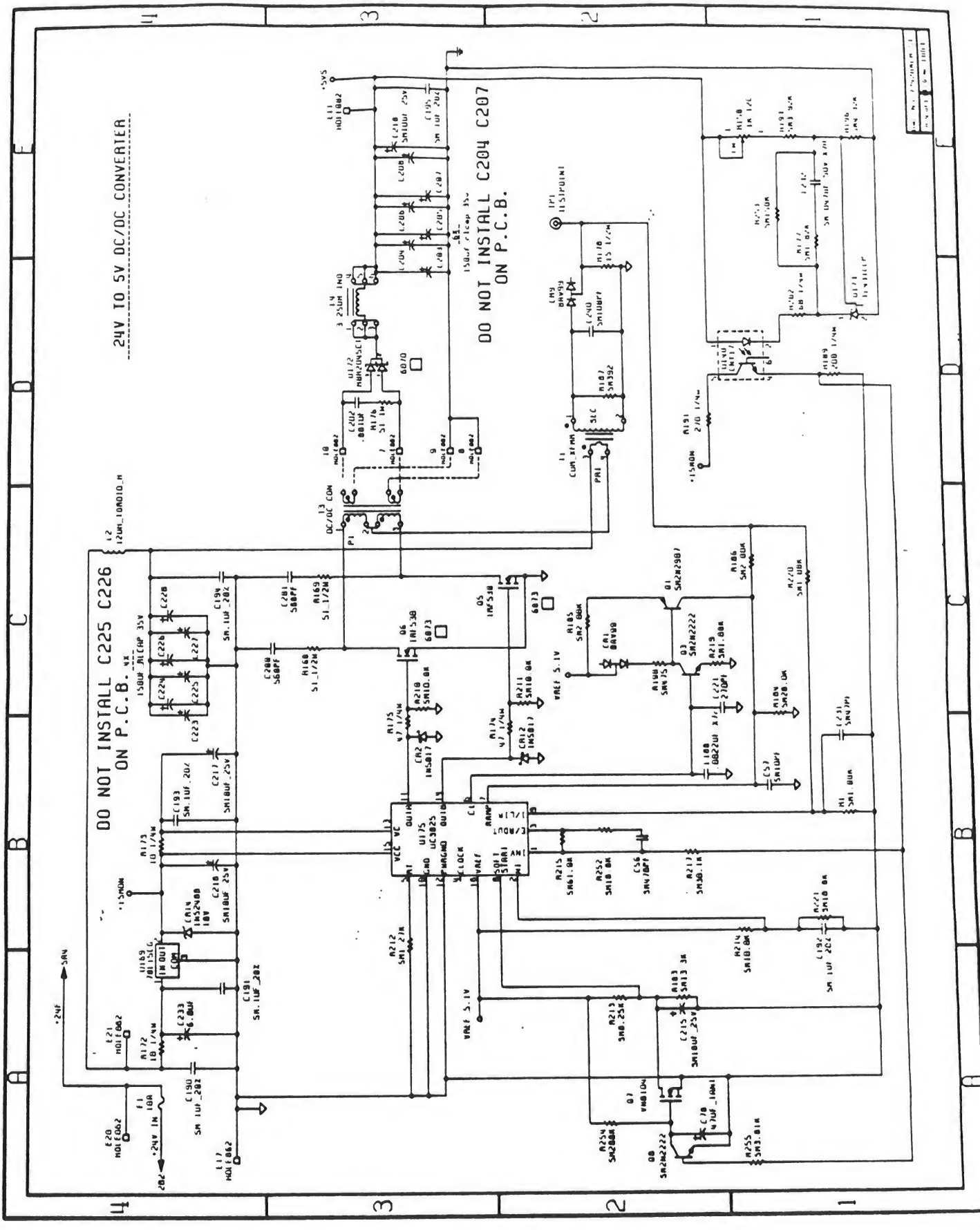
7242AMP **Sheet 3.**

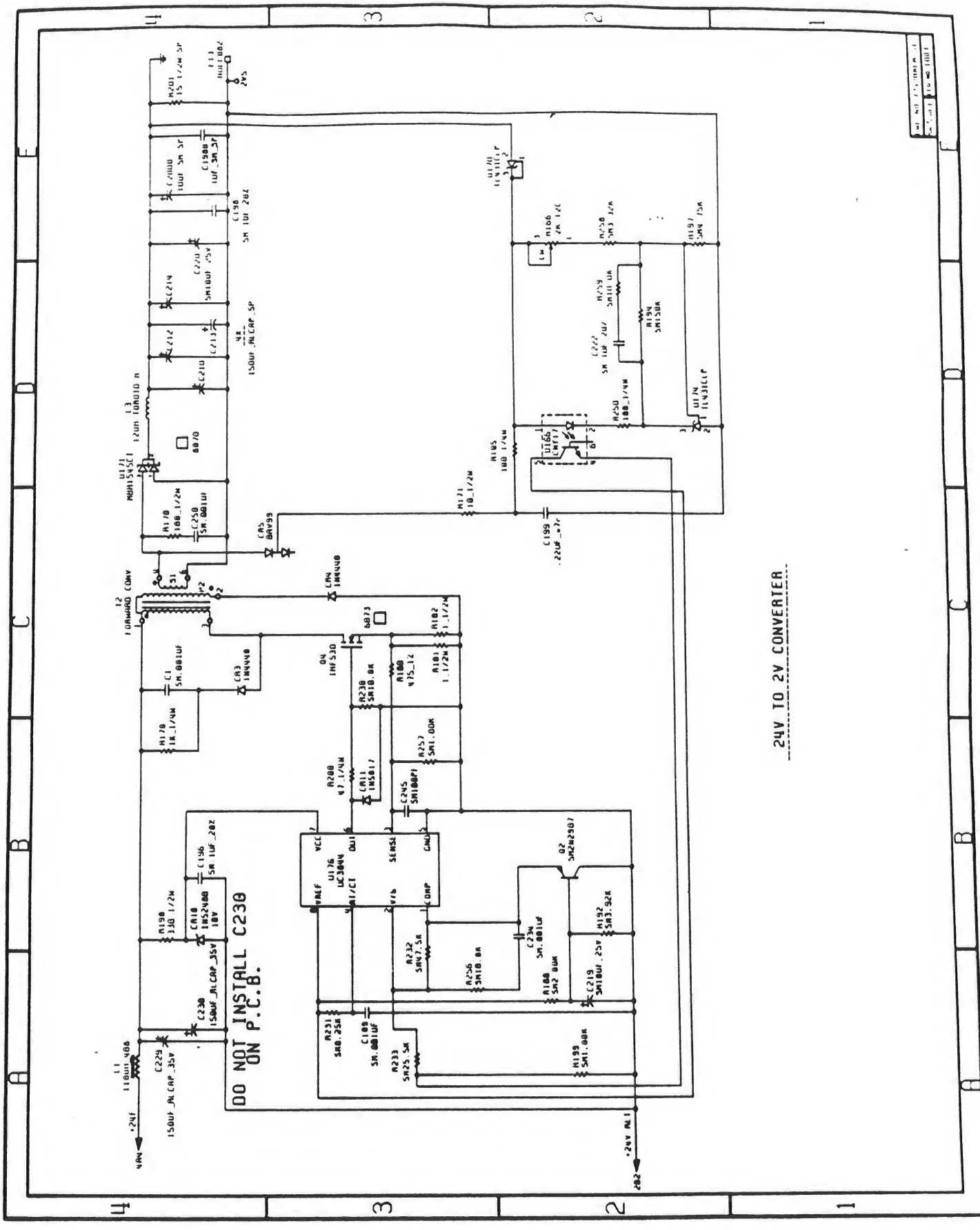


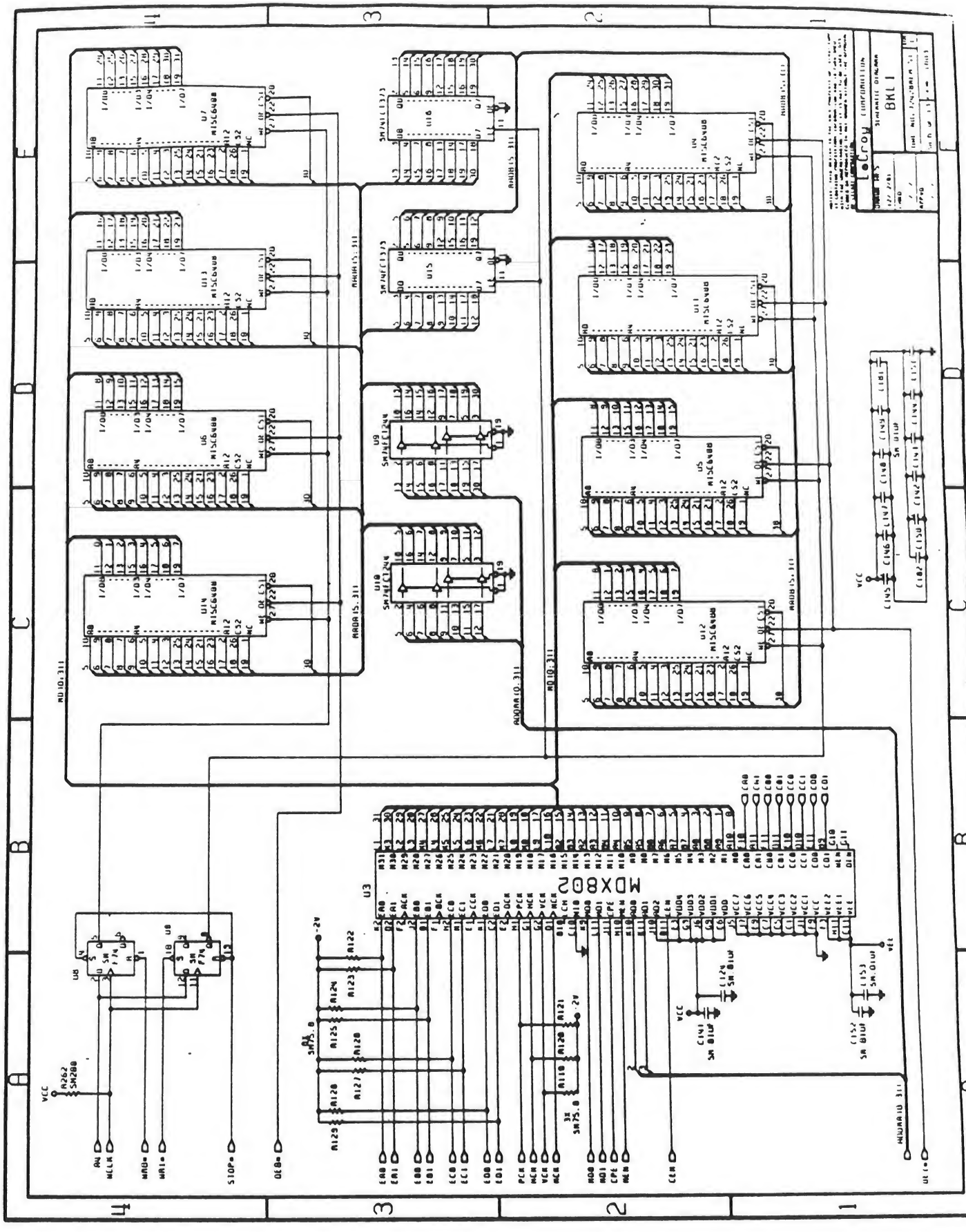


7242BMEM **Sheet 2.**

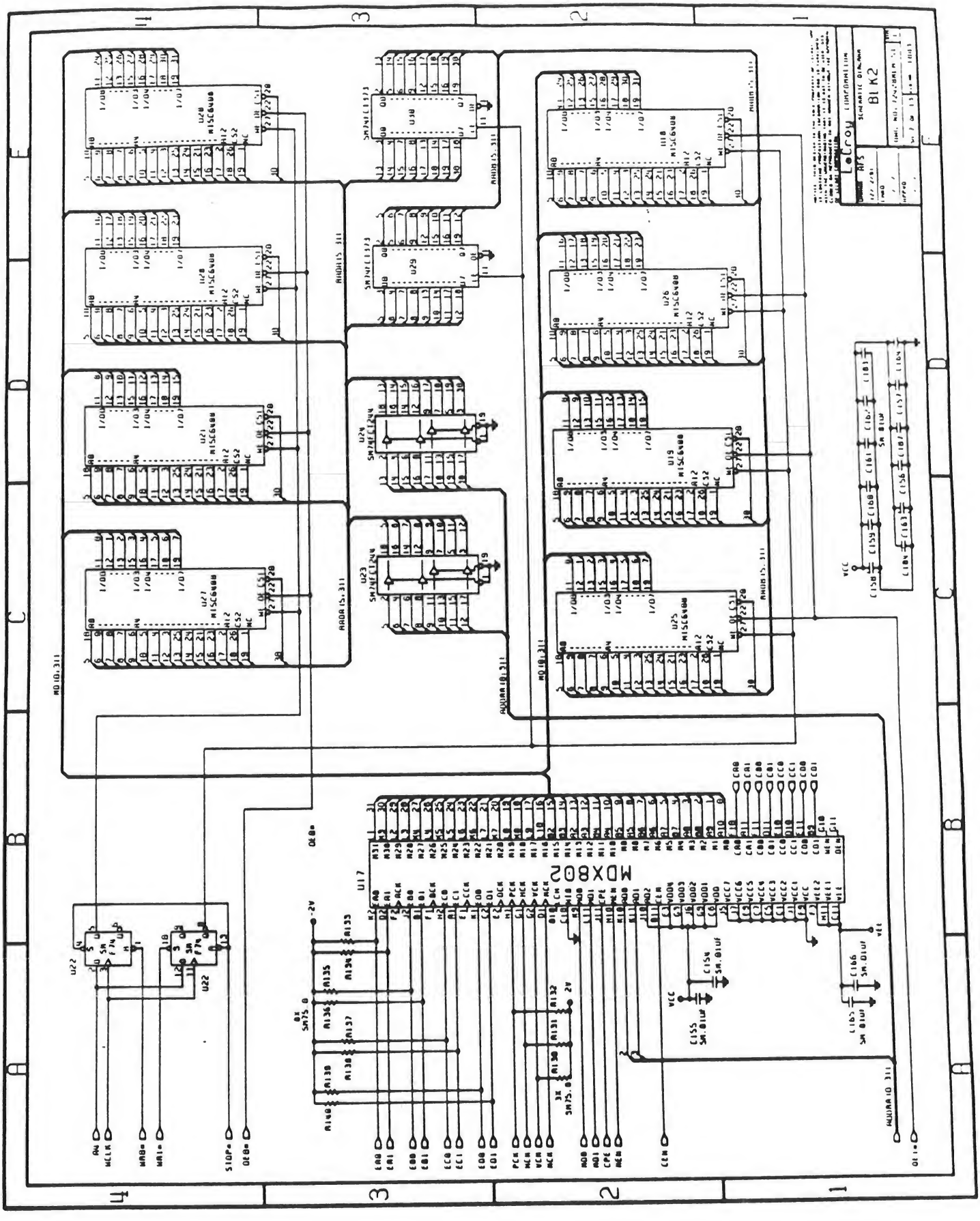

DO NOT
INSTALL
R1000


24V TO 5V DC/DC CONVERTER
DO NOT INSTALL C225 C226
ON P.C.B.
DO NOT INSTALL C204 C207
ON P.C.B.

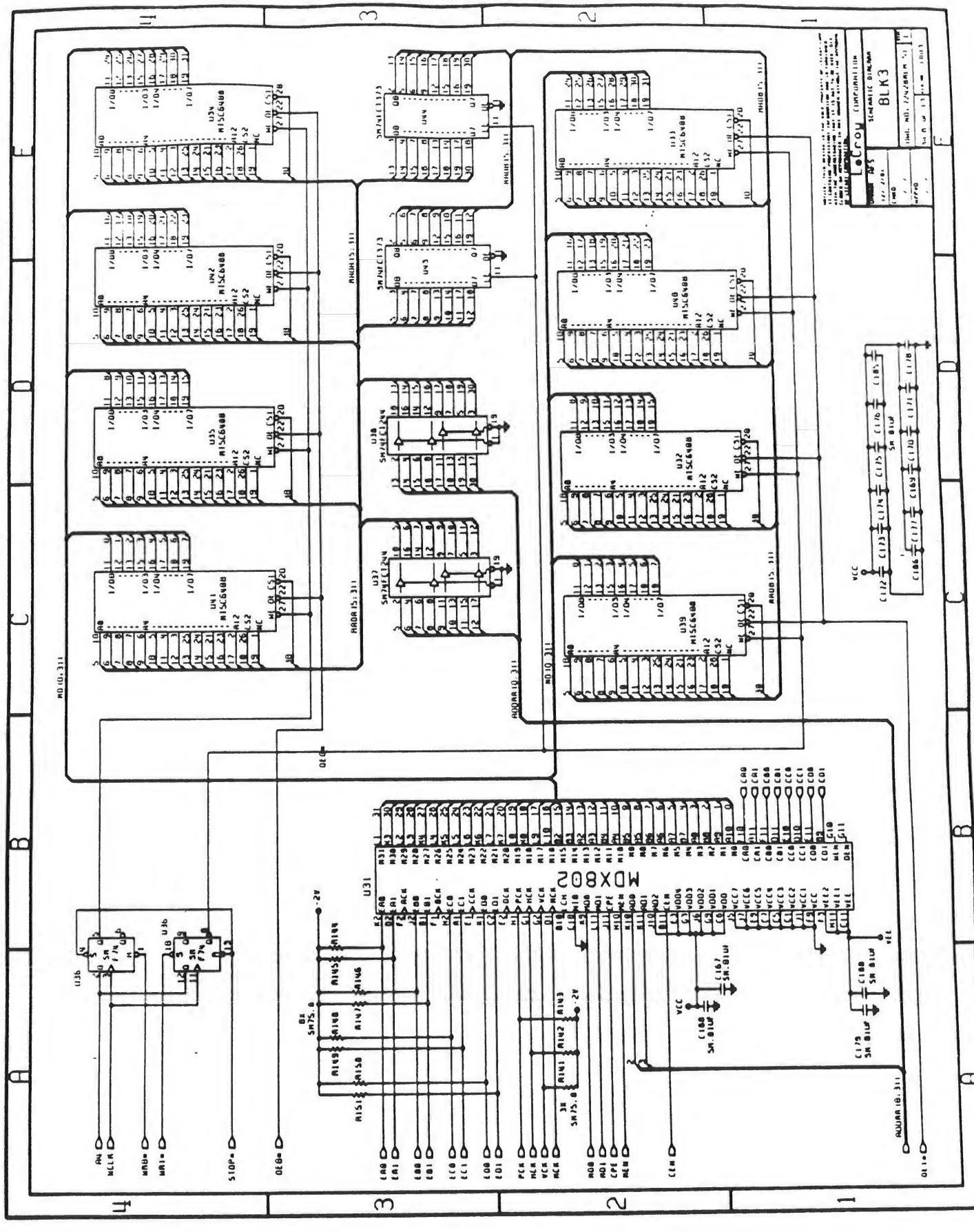

24V TO 2V CONVERTER
DO NOT INSTALL C230
ON P.C.B.



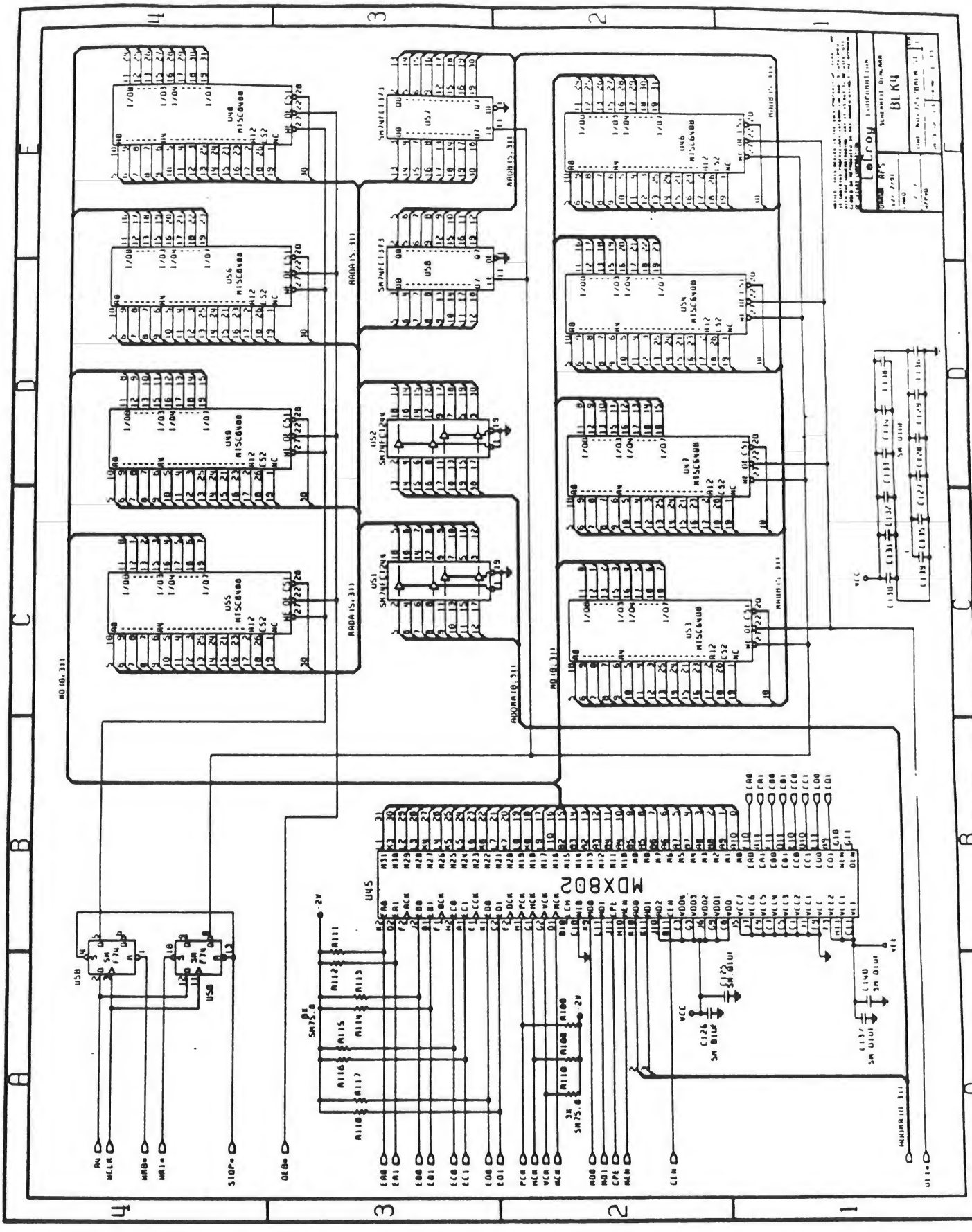
7242BMEM **Sheet 6.**



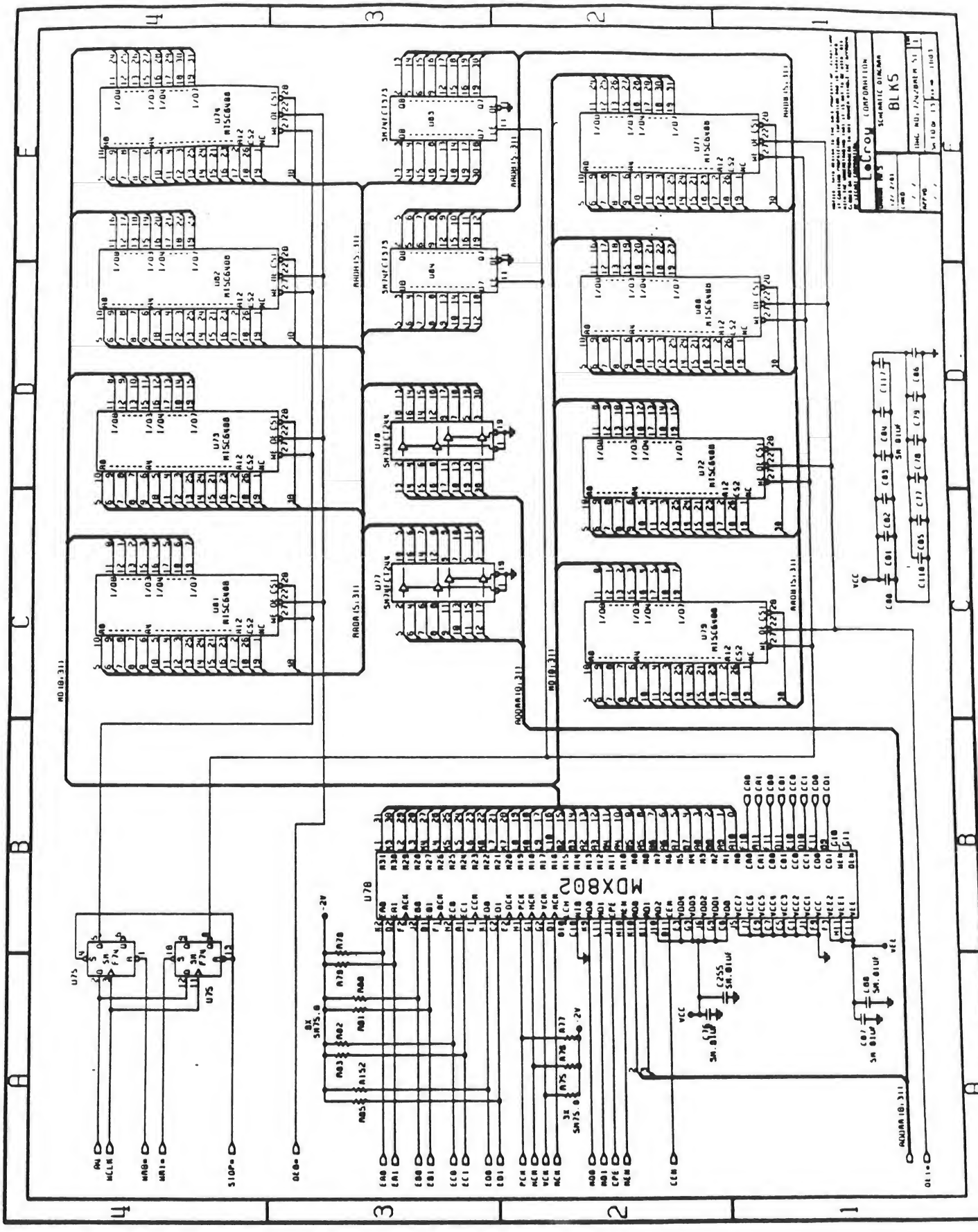
7242BMEM **Sheet 7.**



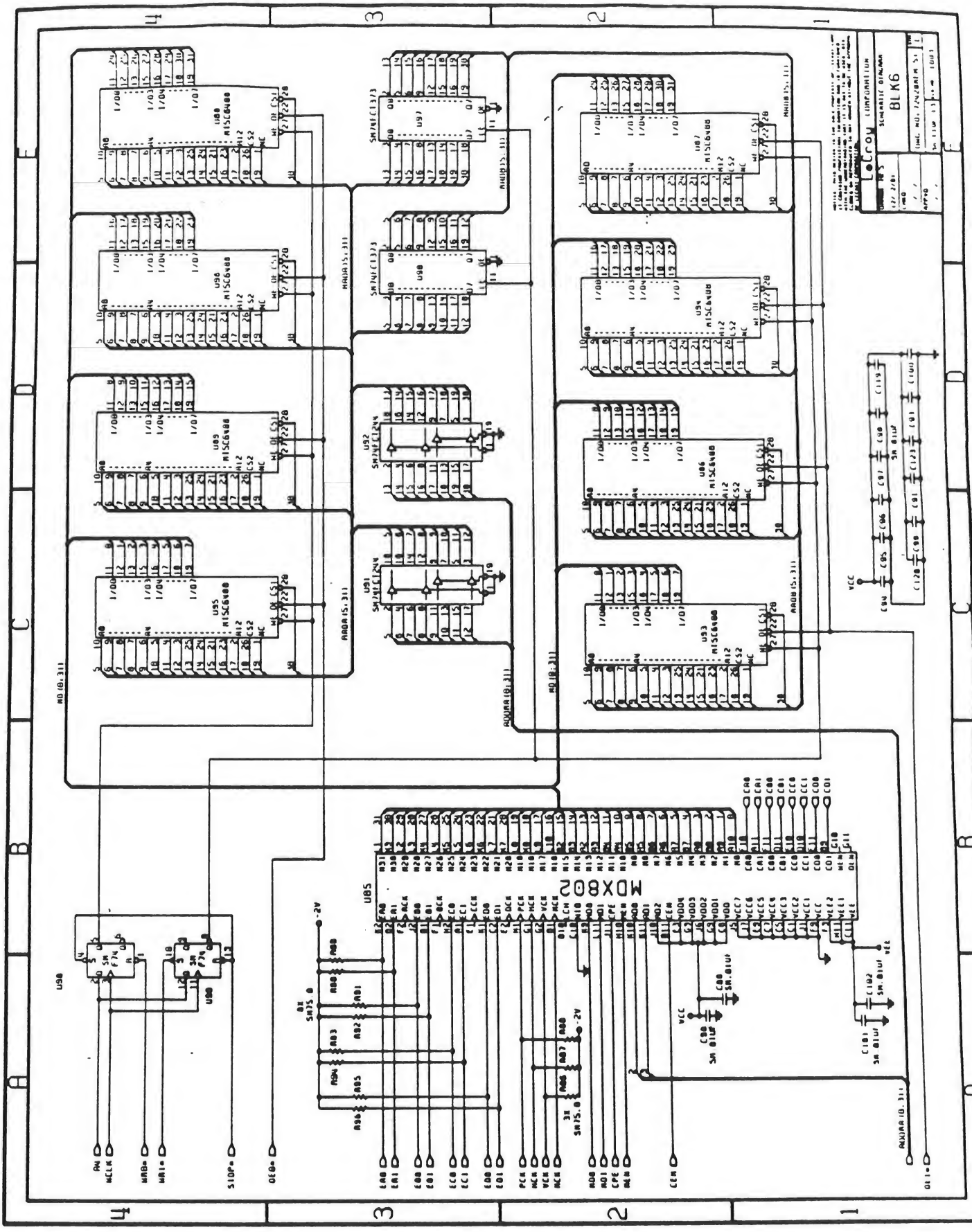
7242BMEM **Sheet 8.**



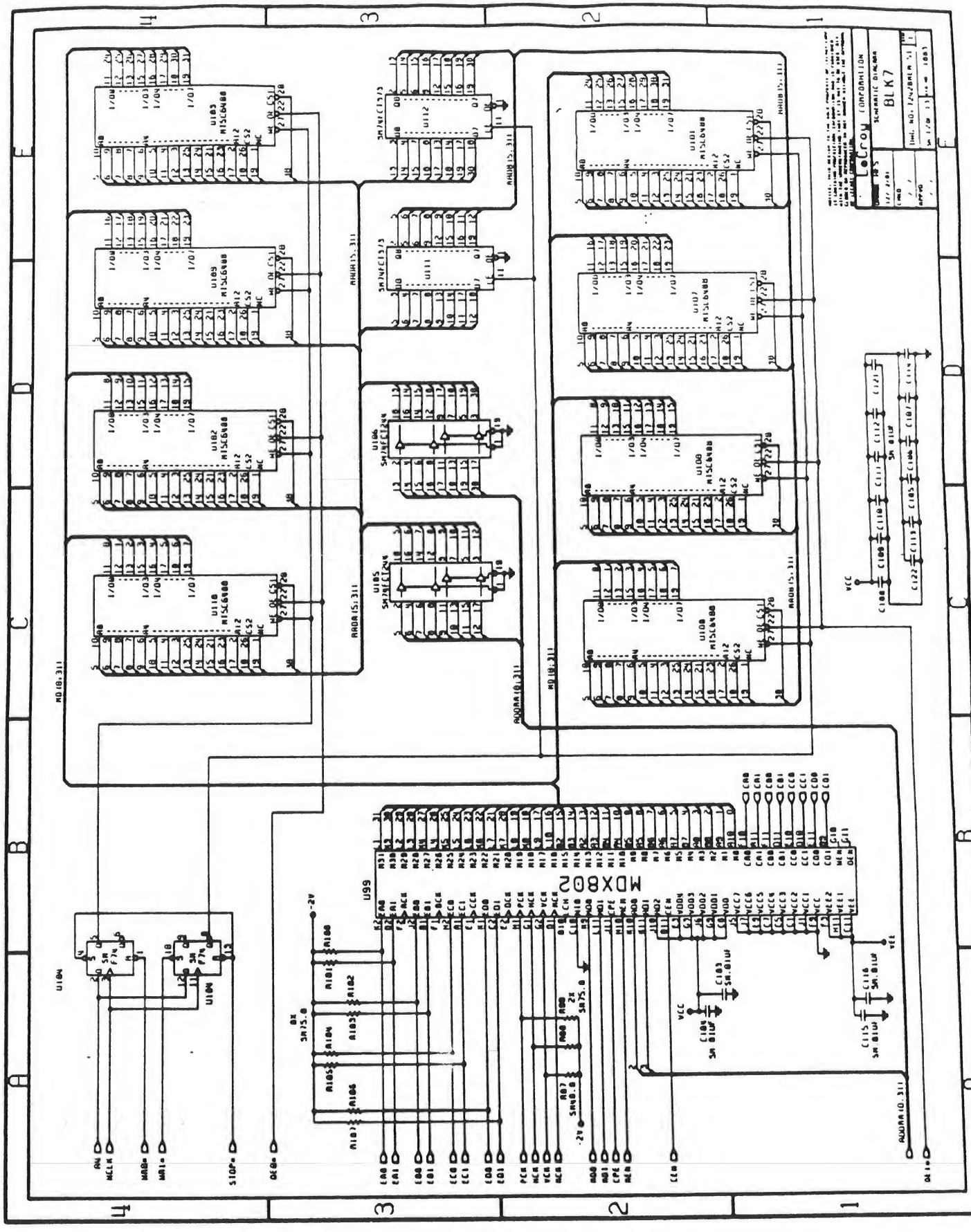
7242BMEM **Sheet 9.**



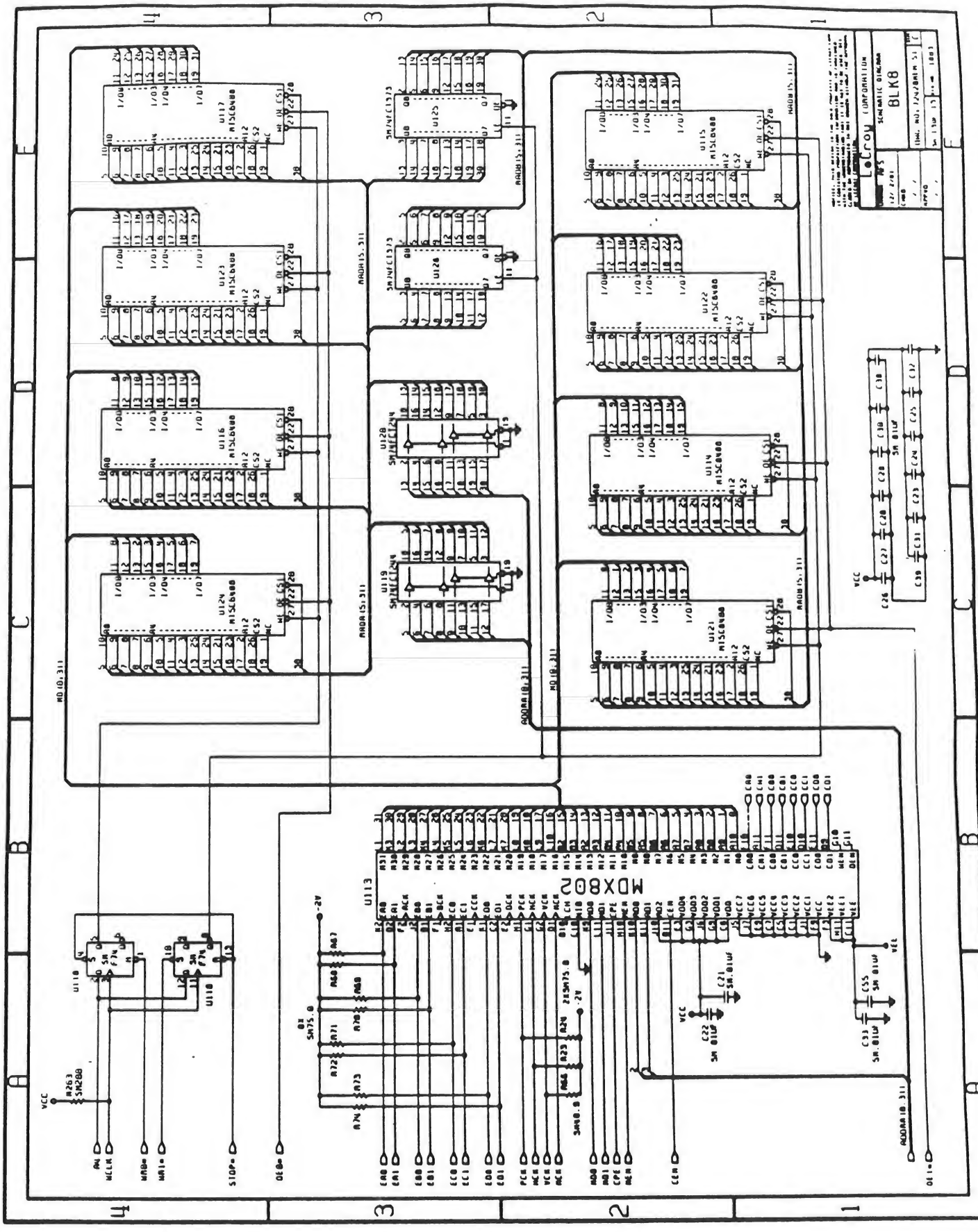
7242BMEM **Sheet 10.**

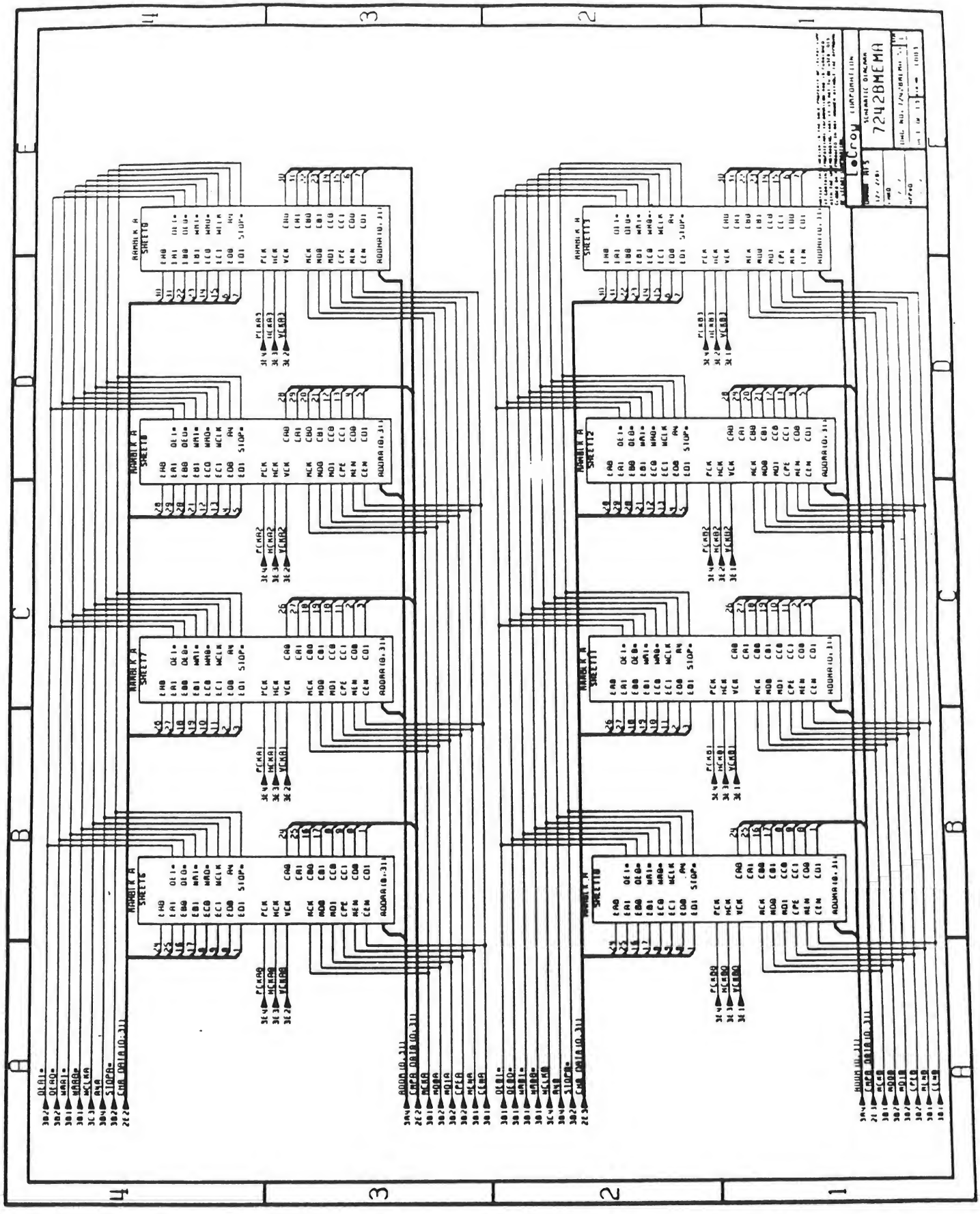


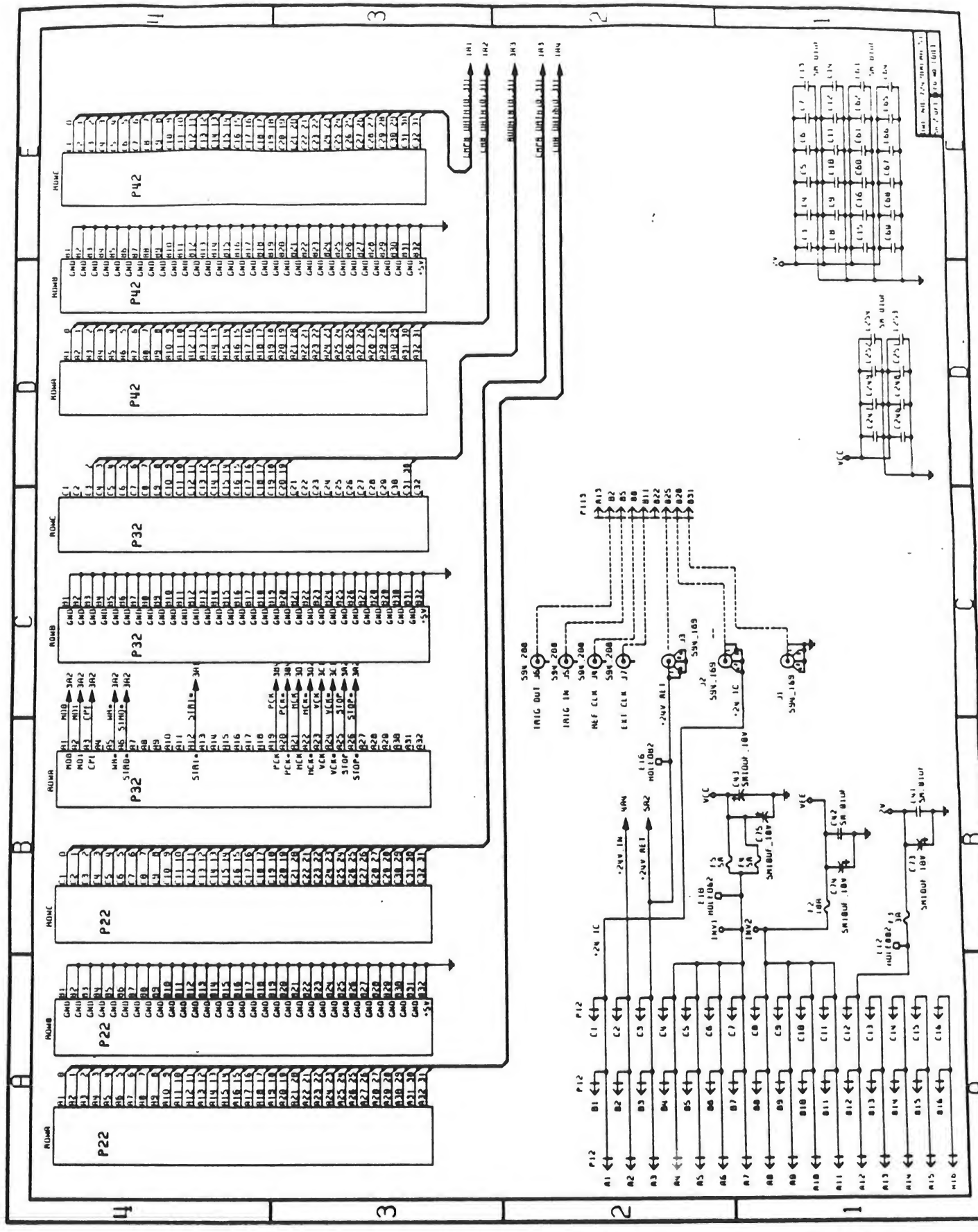
7242BMEM **Sheet 11.**

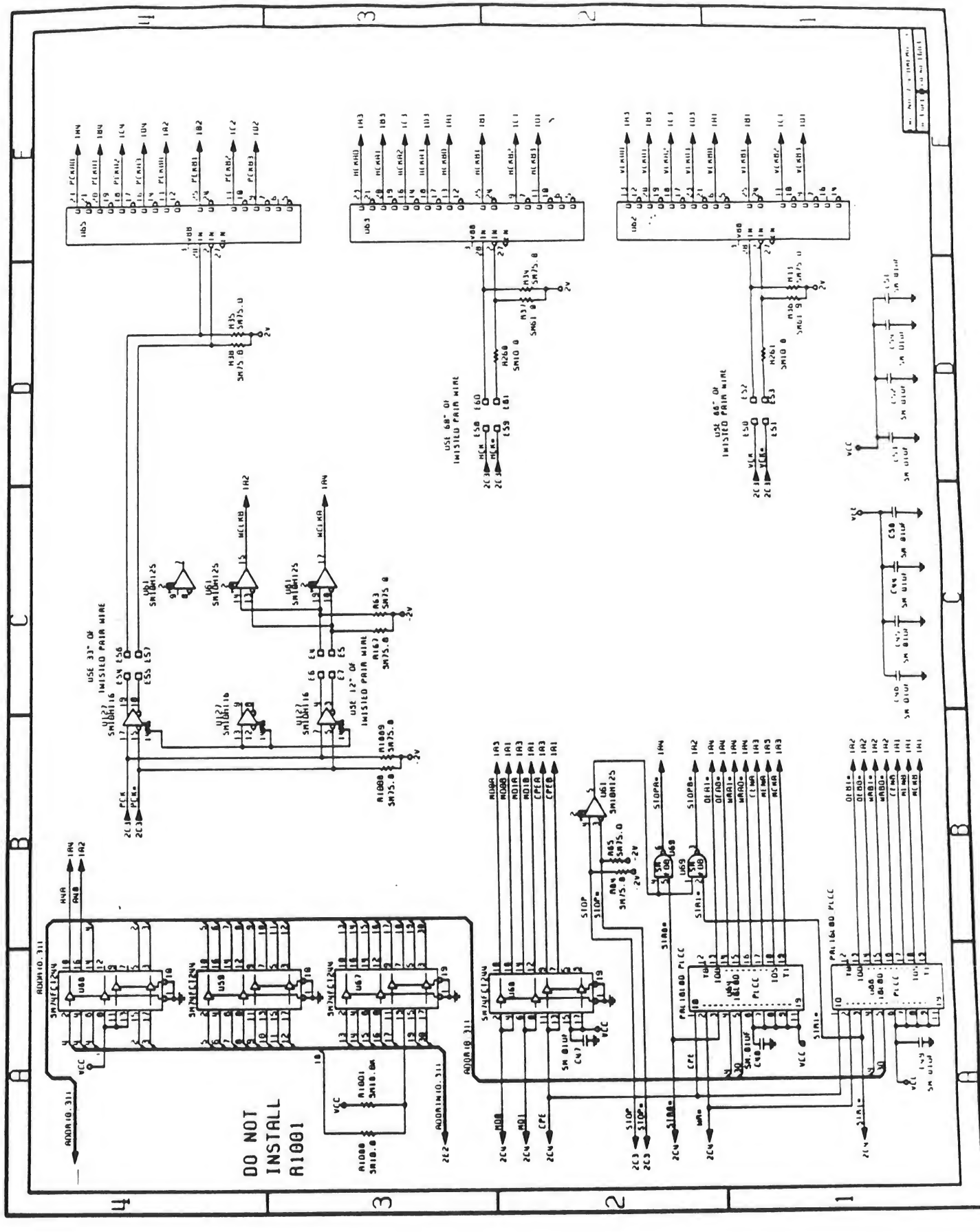


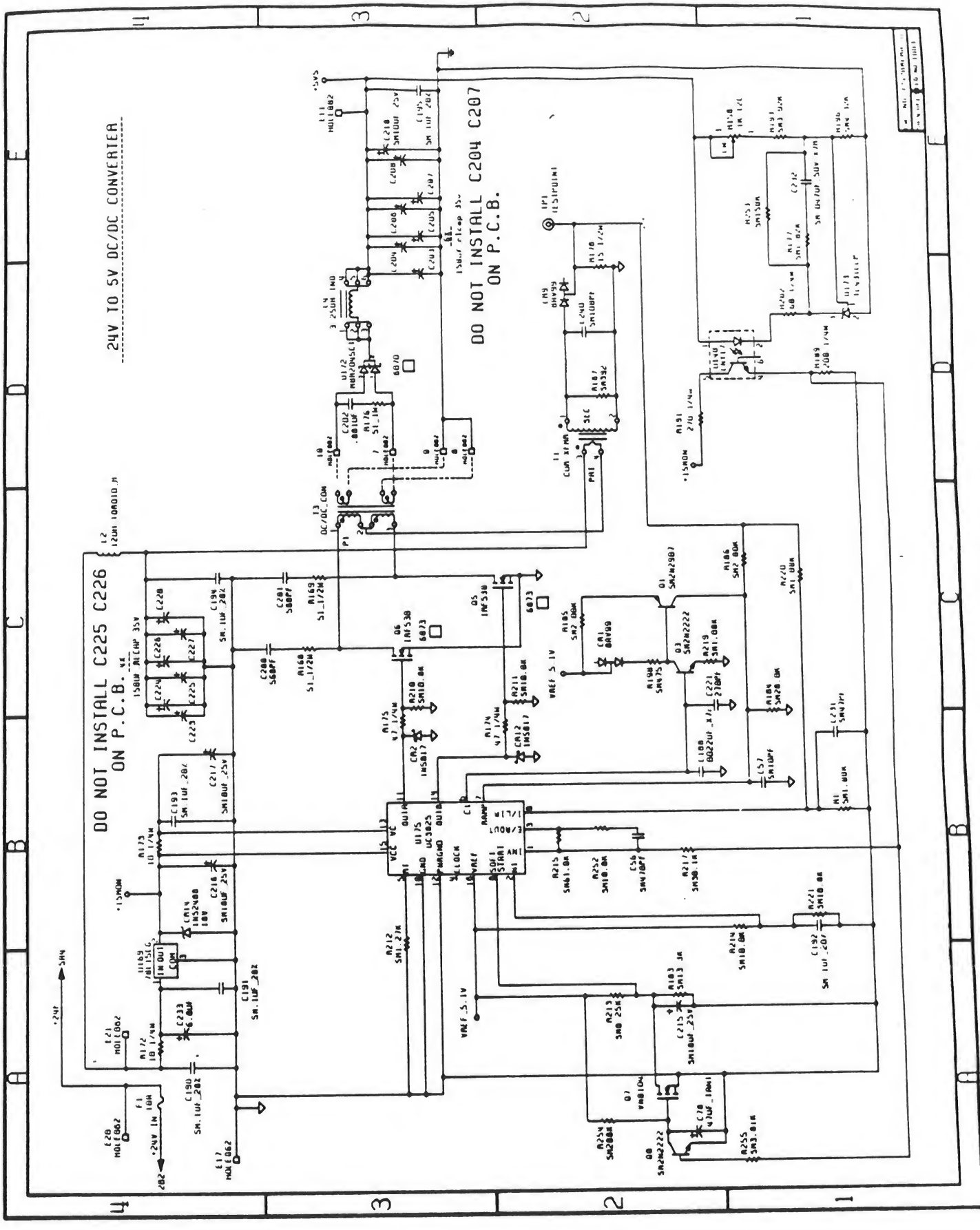
7242BMEM **Sheet 12.**

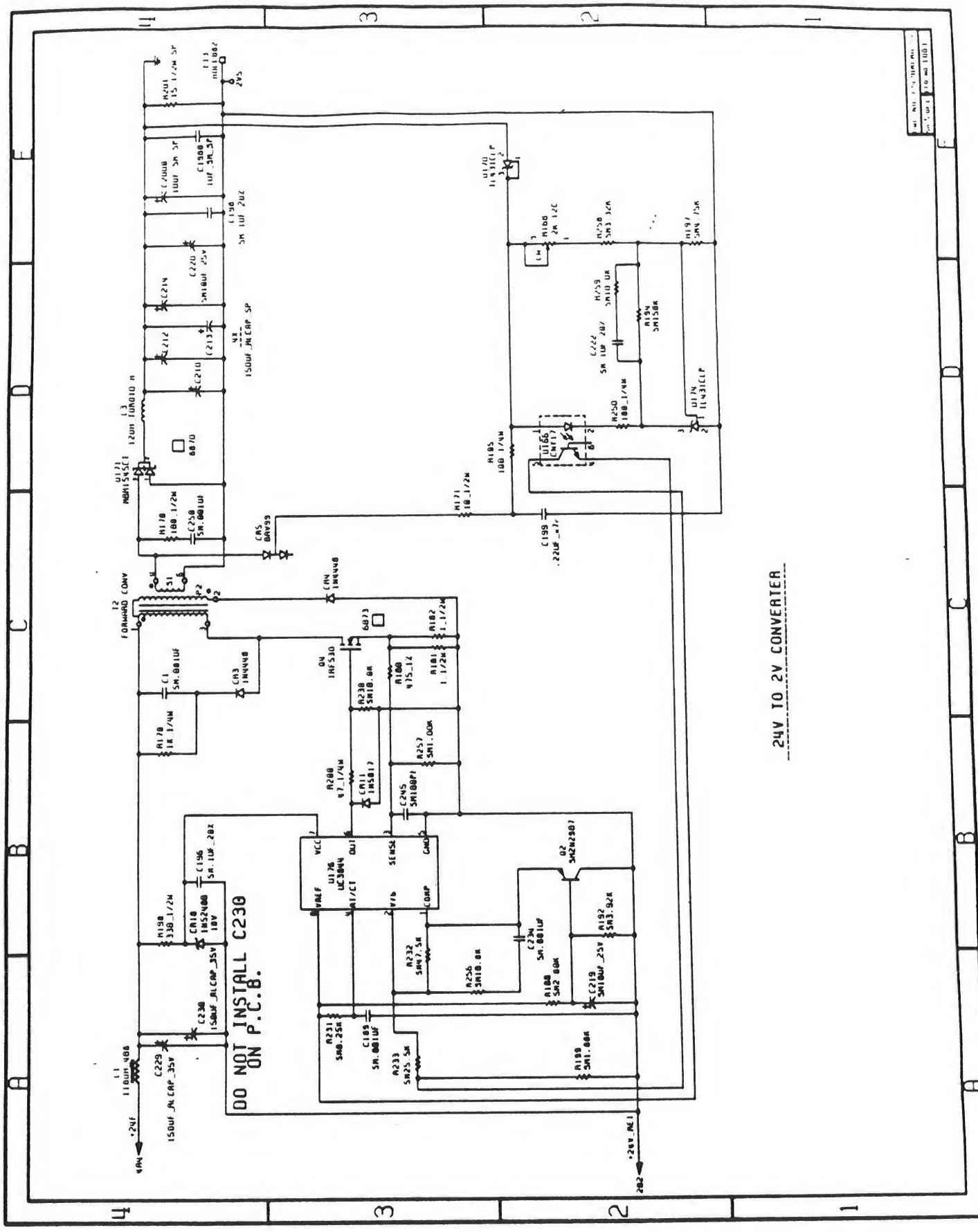

BLK8
MDX802

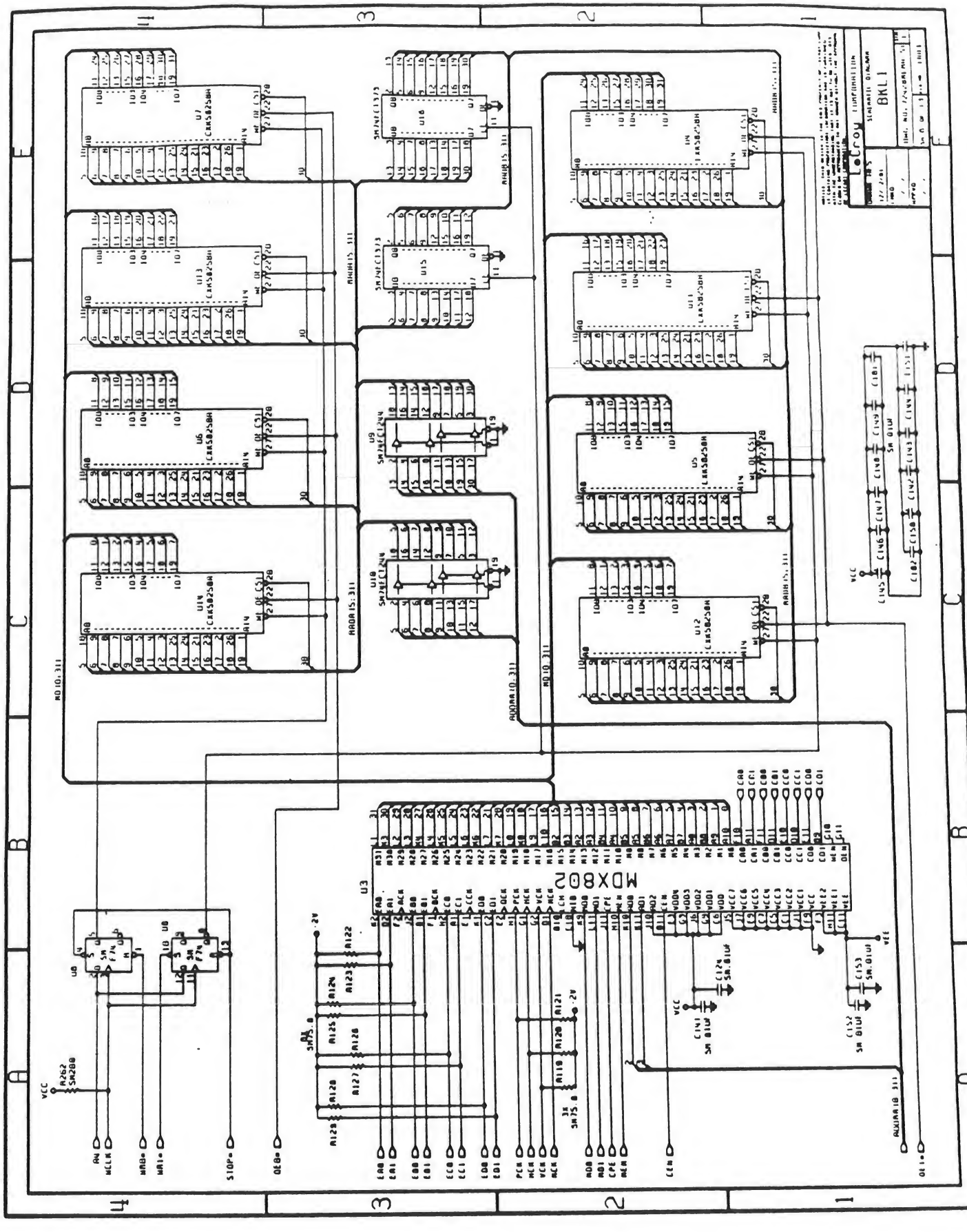




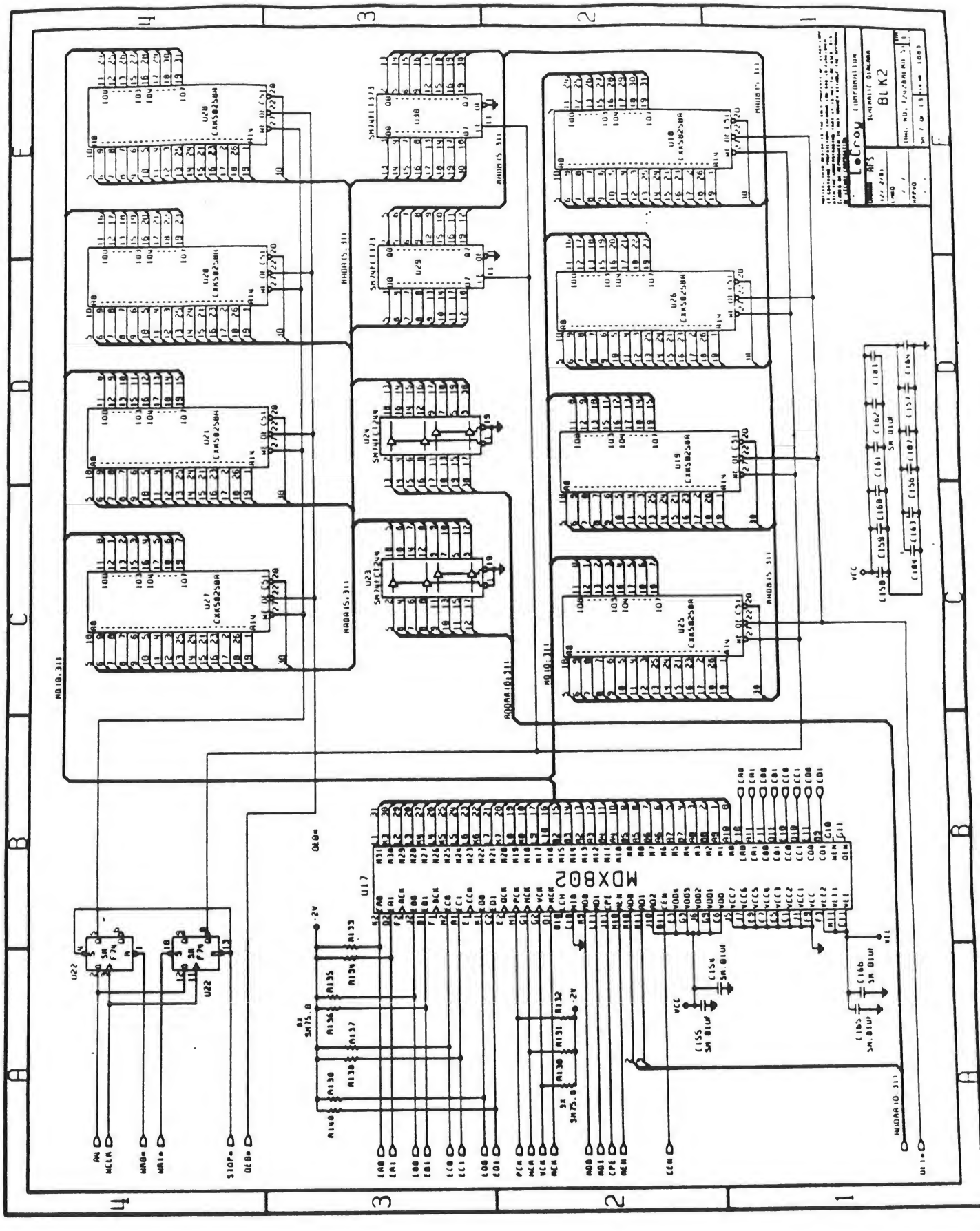

DO NOT
INSTALL
R1001

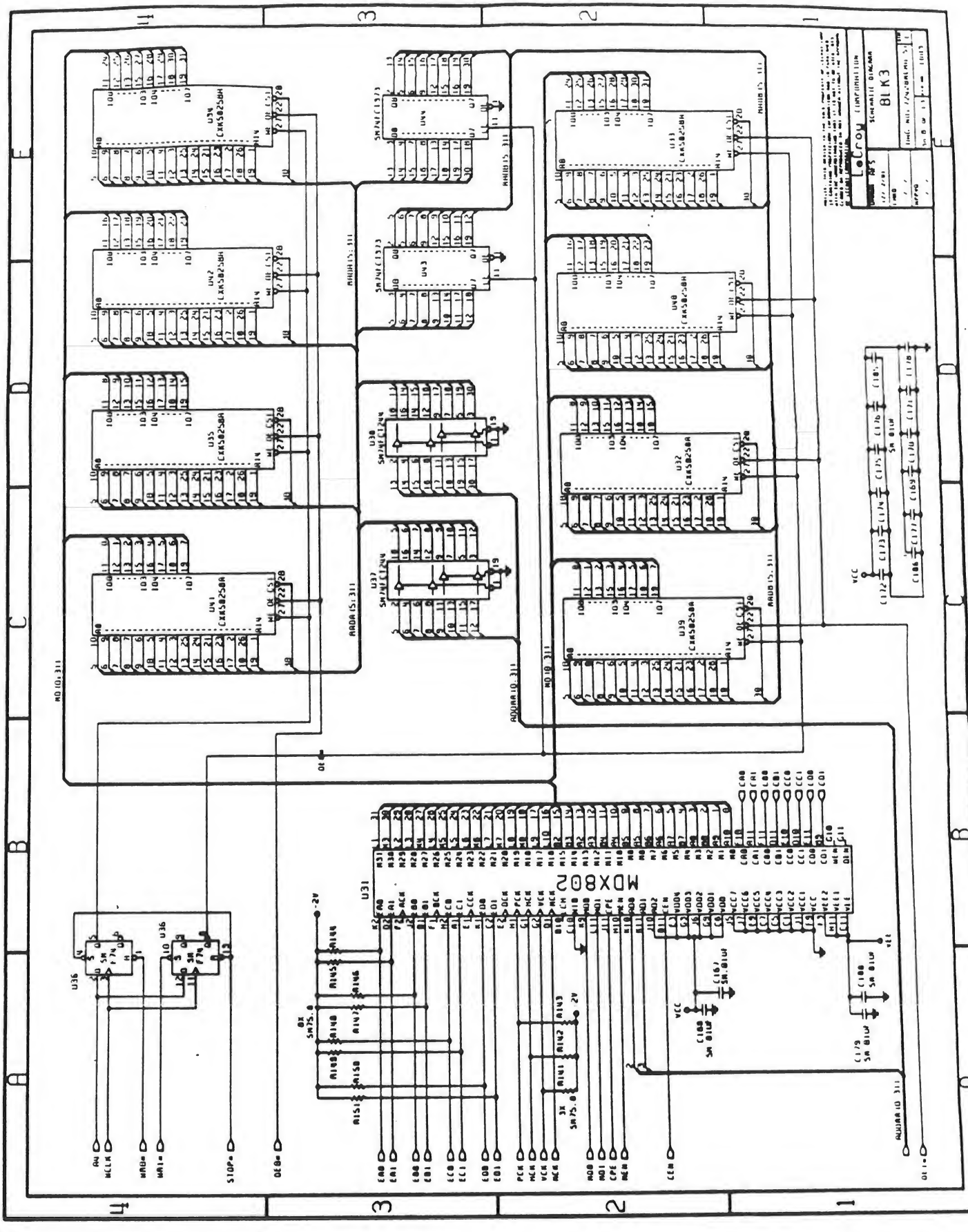

24V TO 5V DC/DC CONVERTER
DO NOT INSTALL C225 C226
ON P.C.B.
DO NOT INSTALL C204 C207
ON P.C.B.


24V TO 2V CONVERTER
DO NOT INSTALL C230
ON P.C.B.

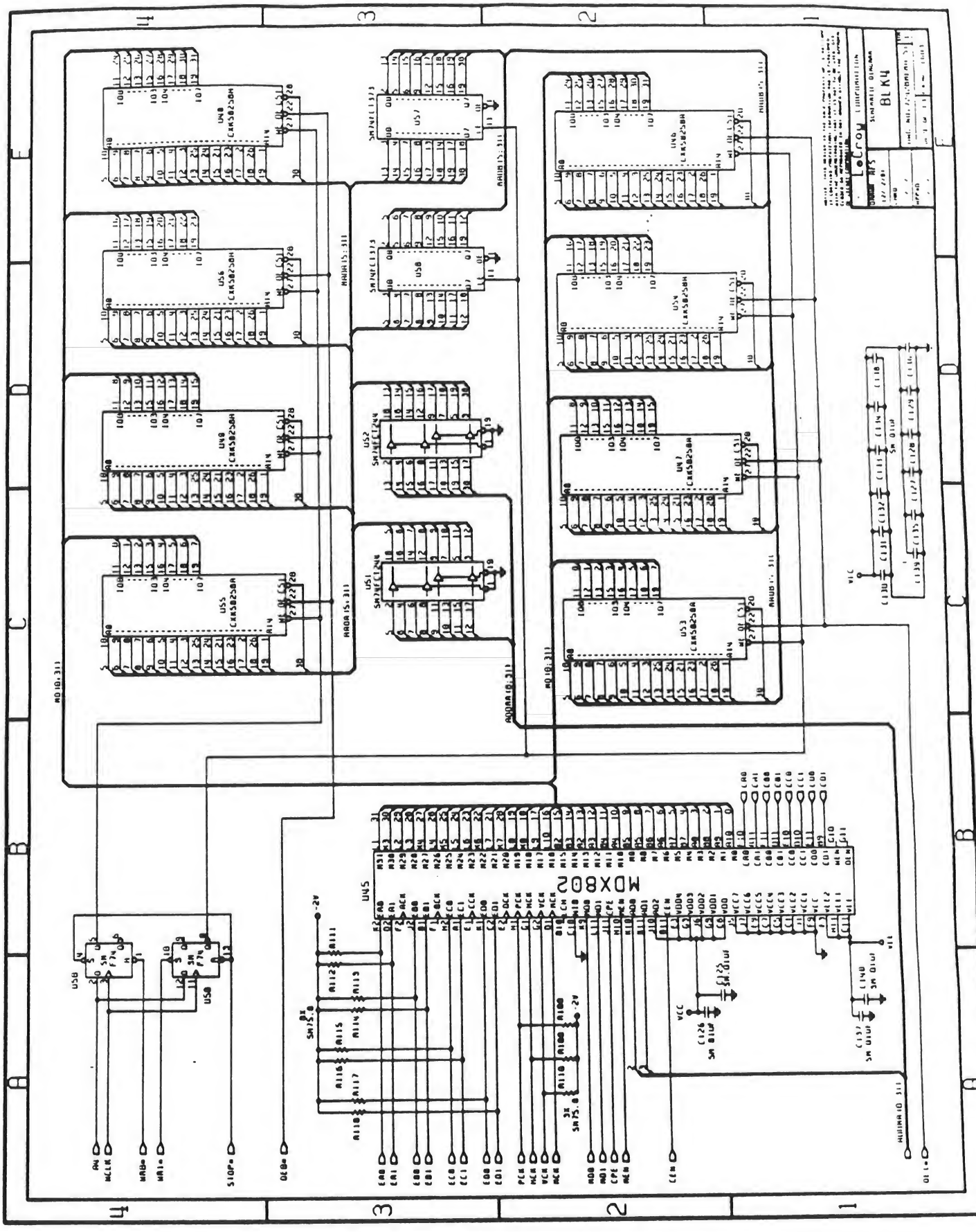


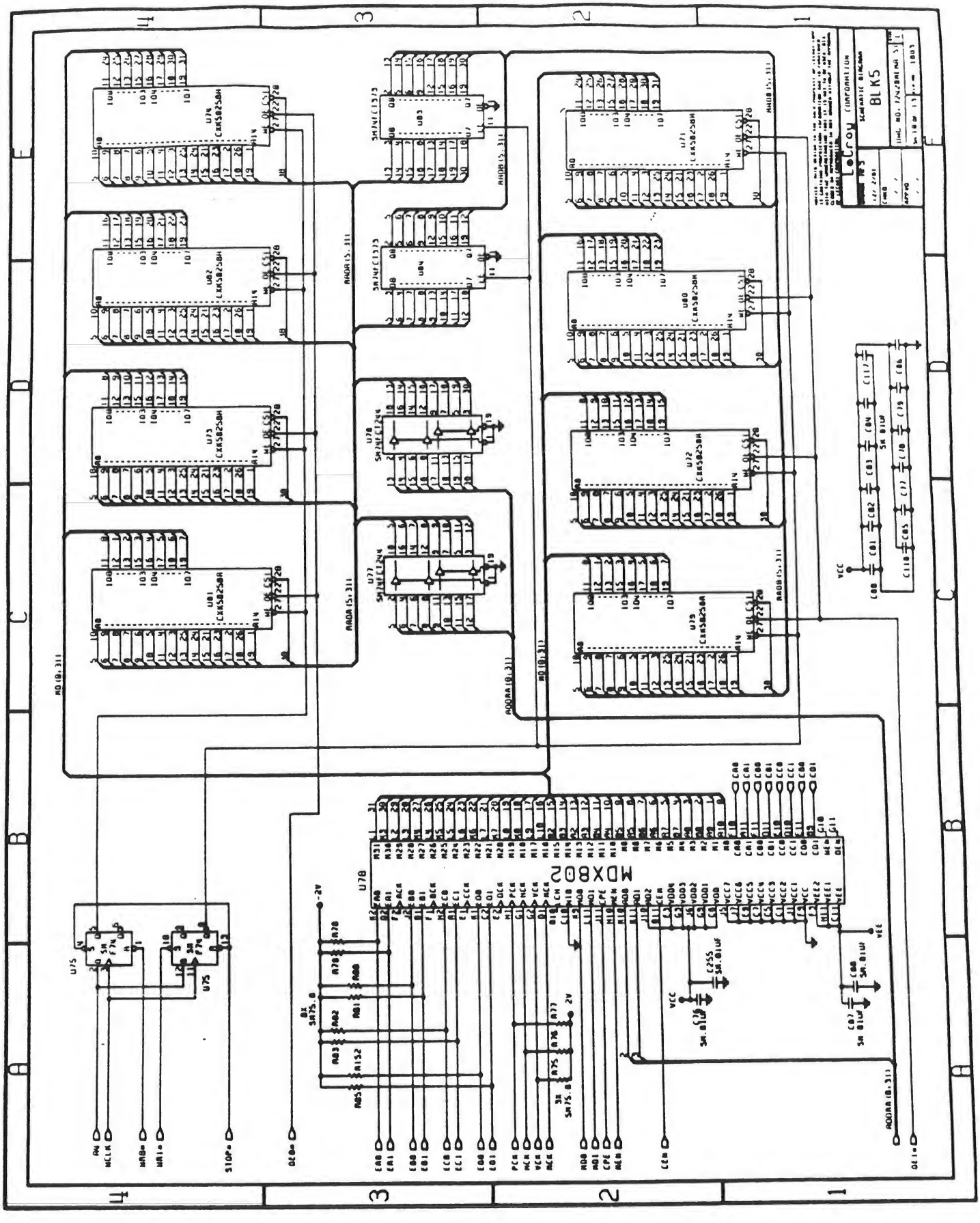
7242BMEMA **Sheet 6.**

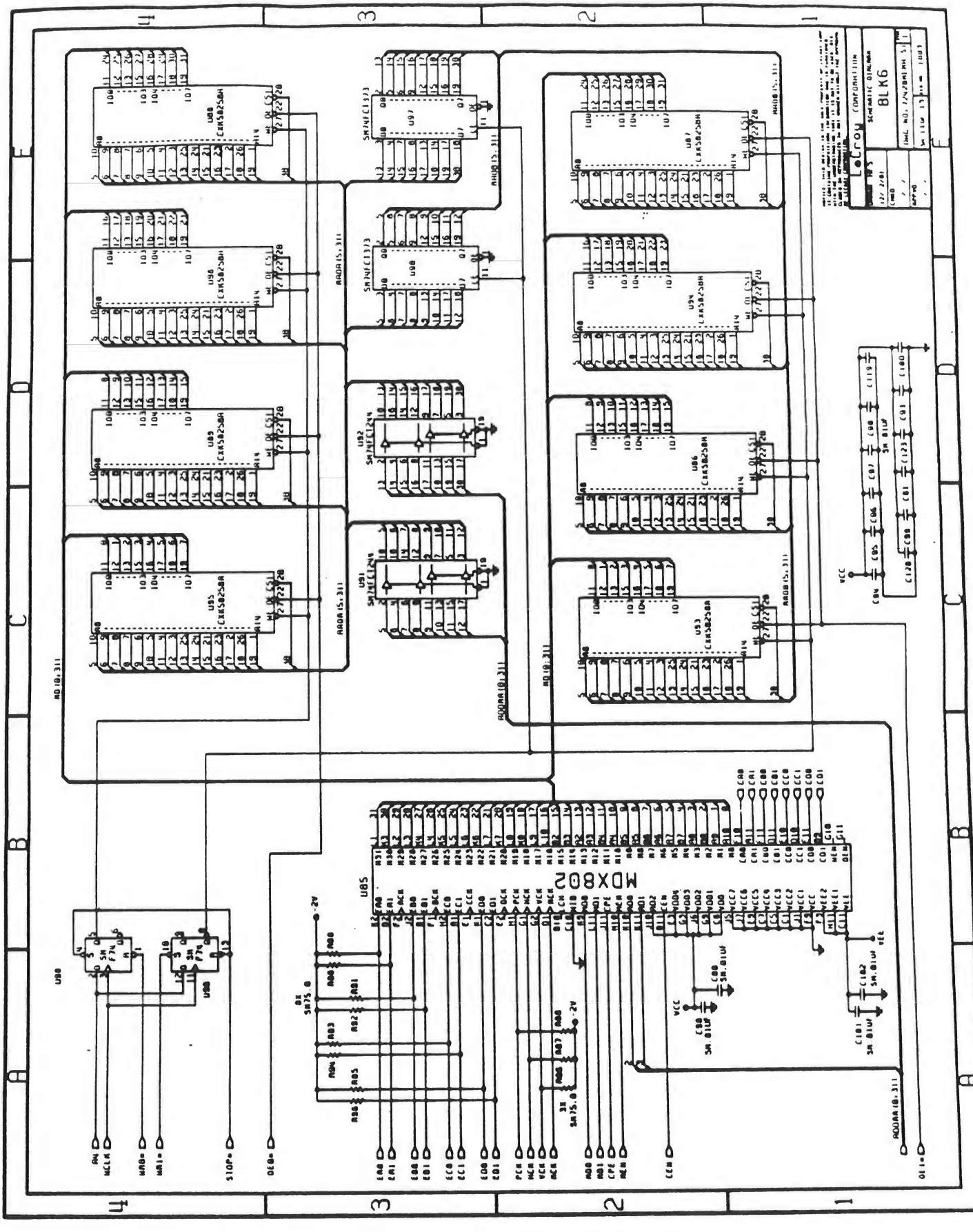




7242BMEMA **Sheet 8.**



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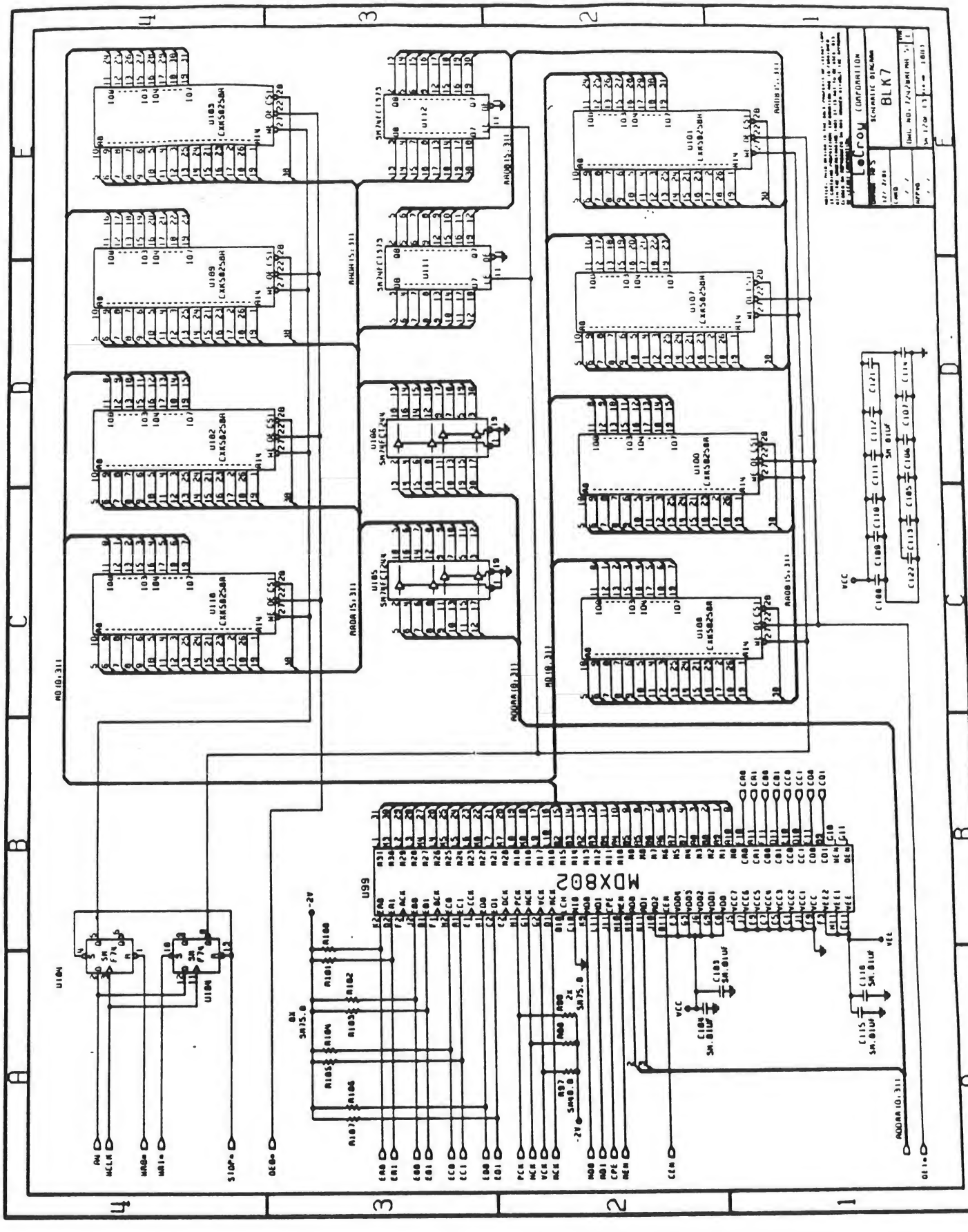
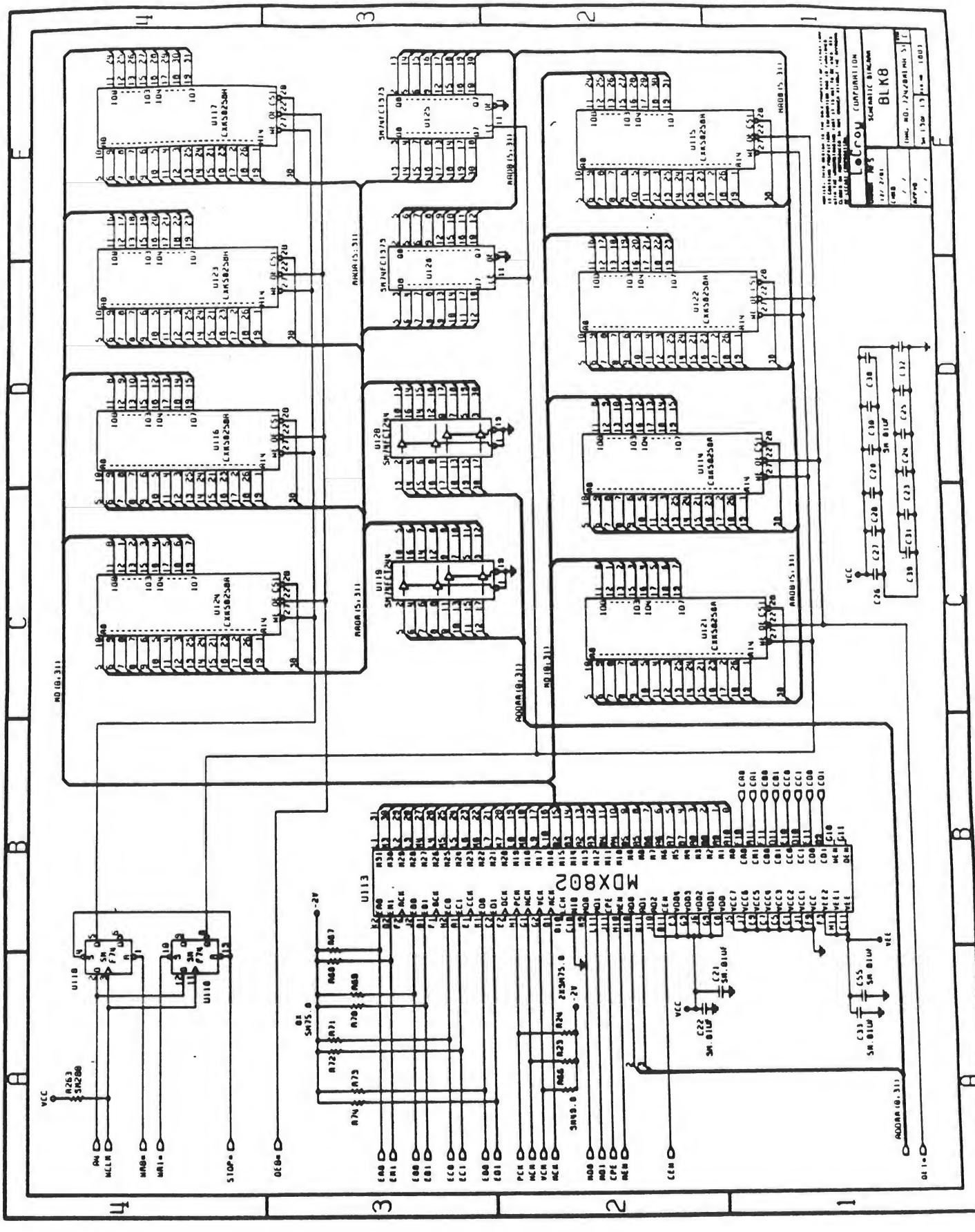
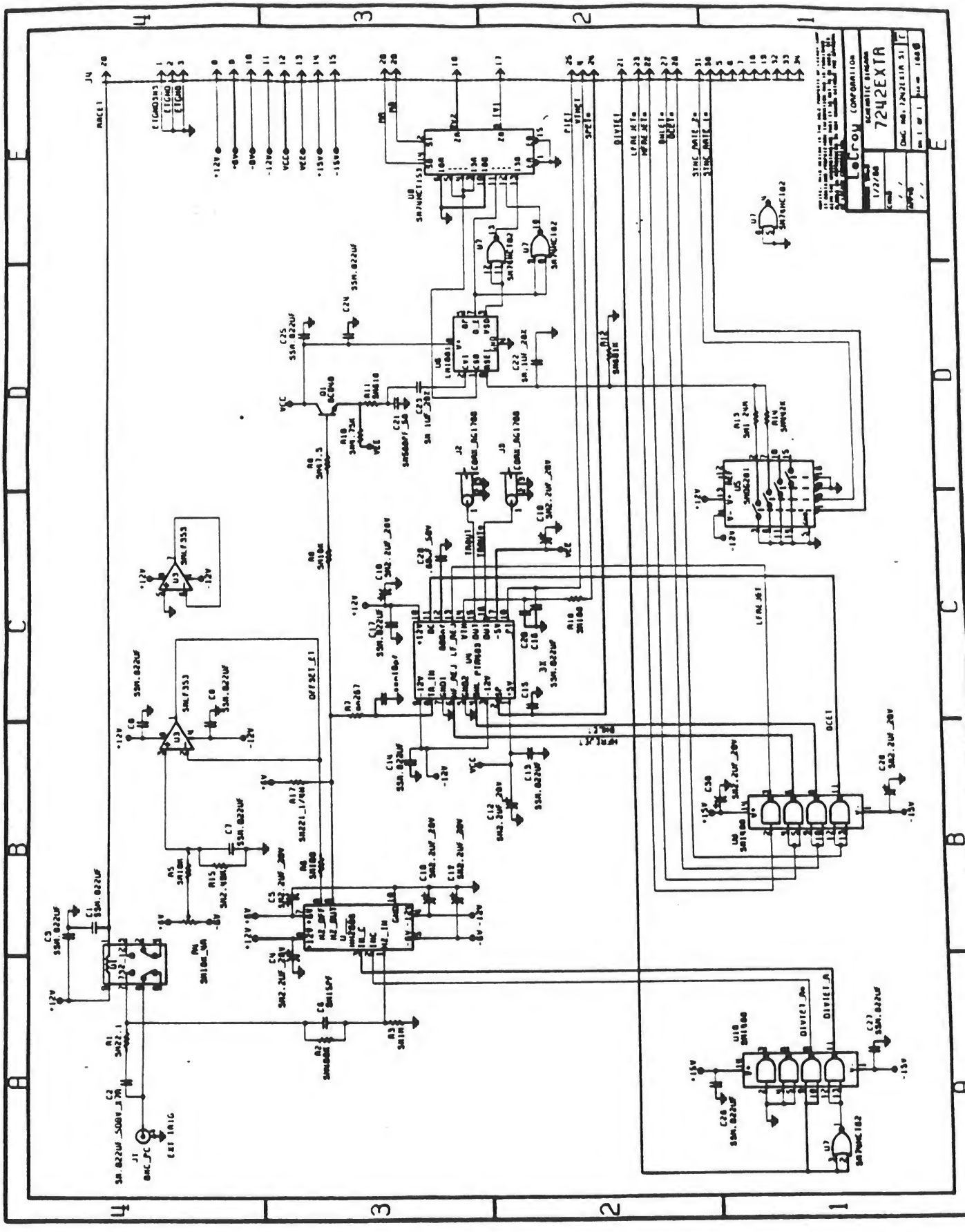
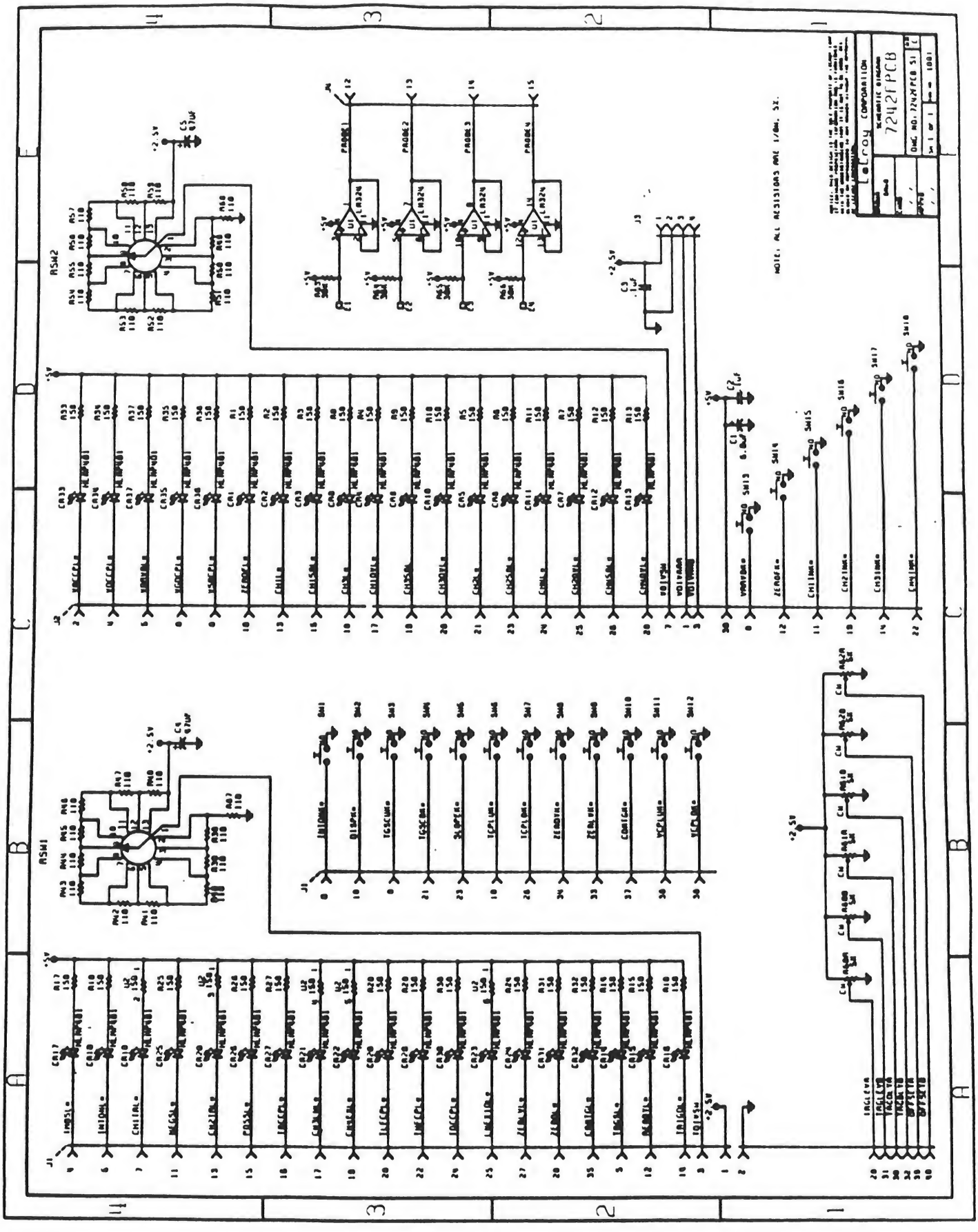
MDX802

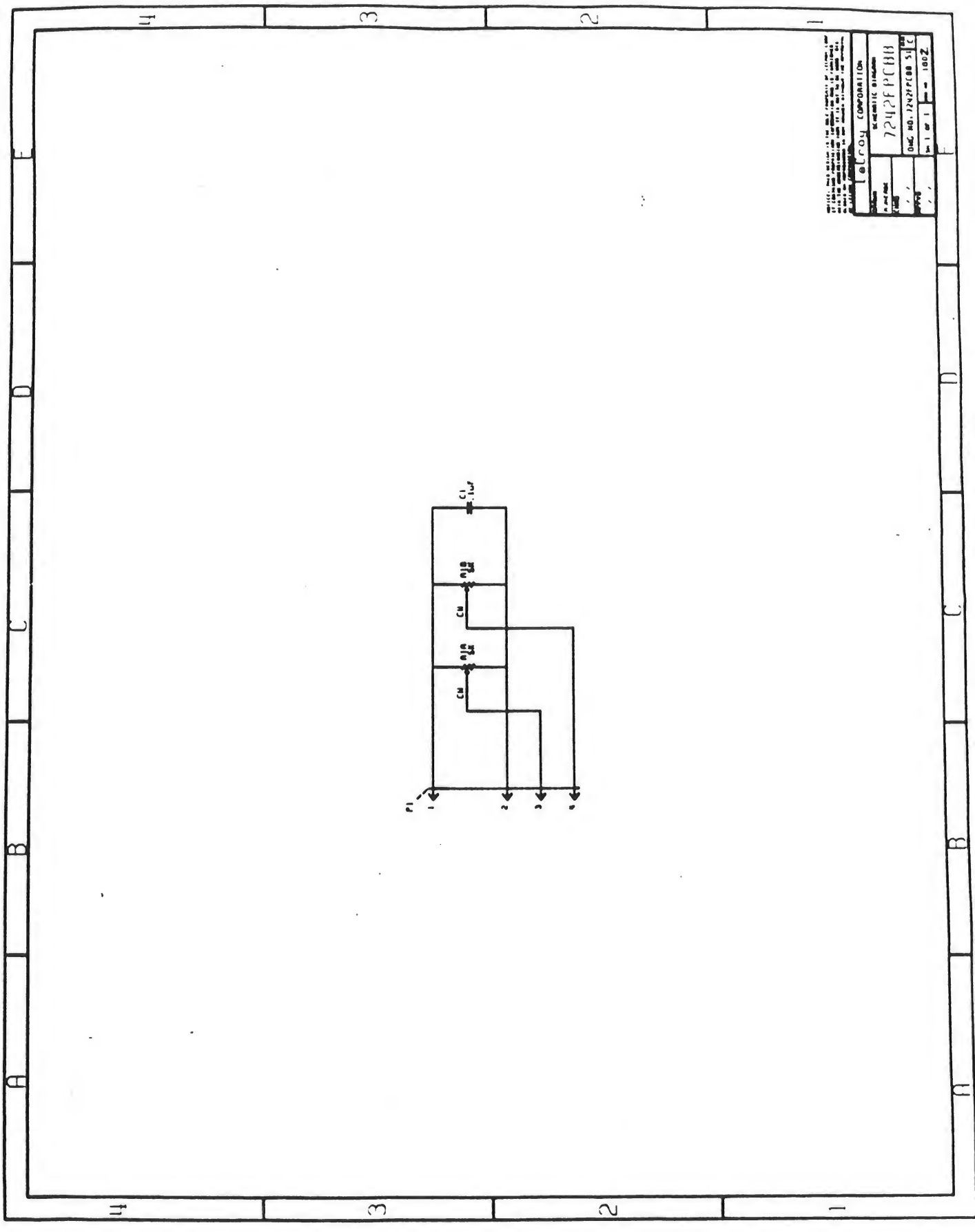


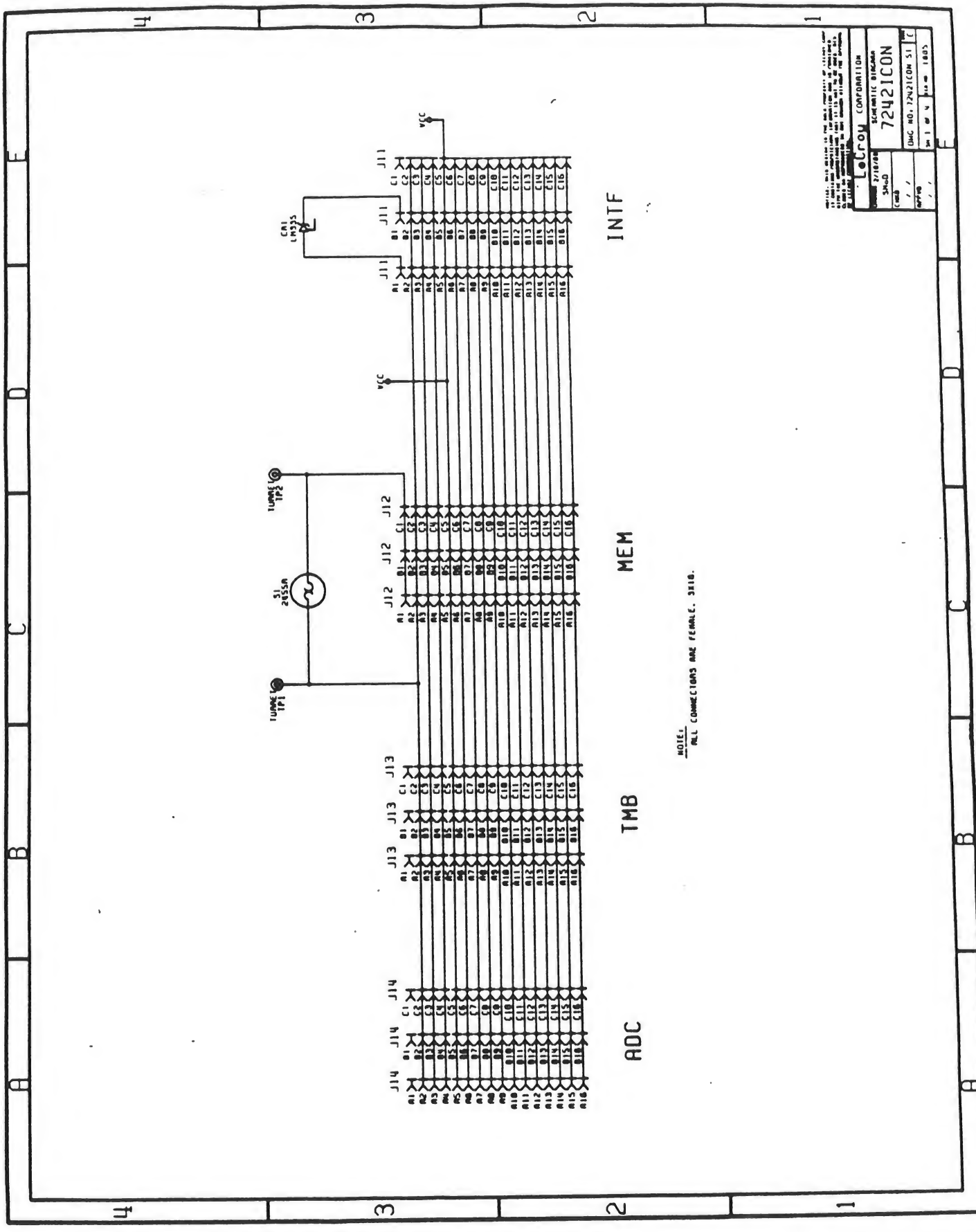


7242BMEMA **Sheet 13.**

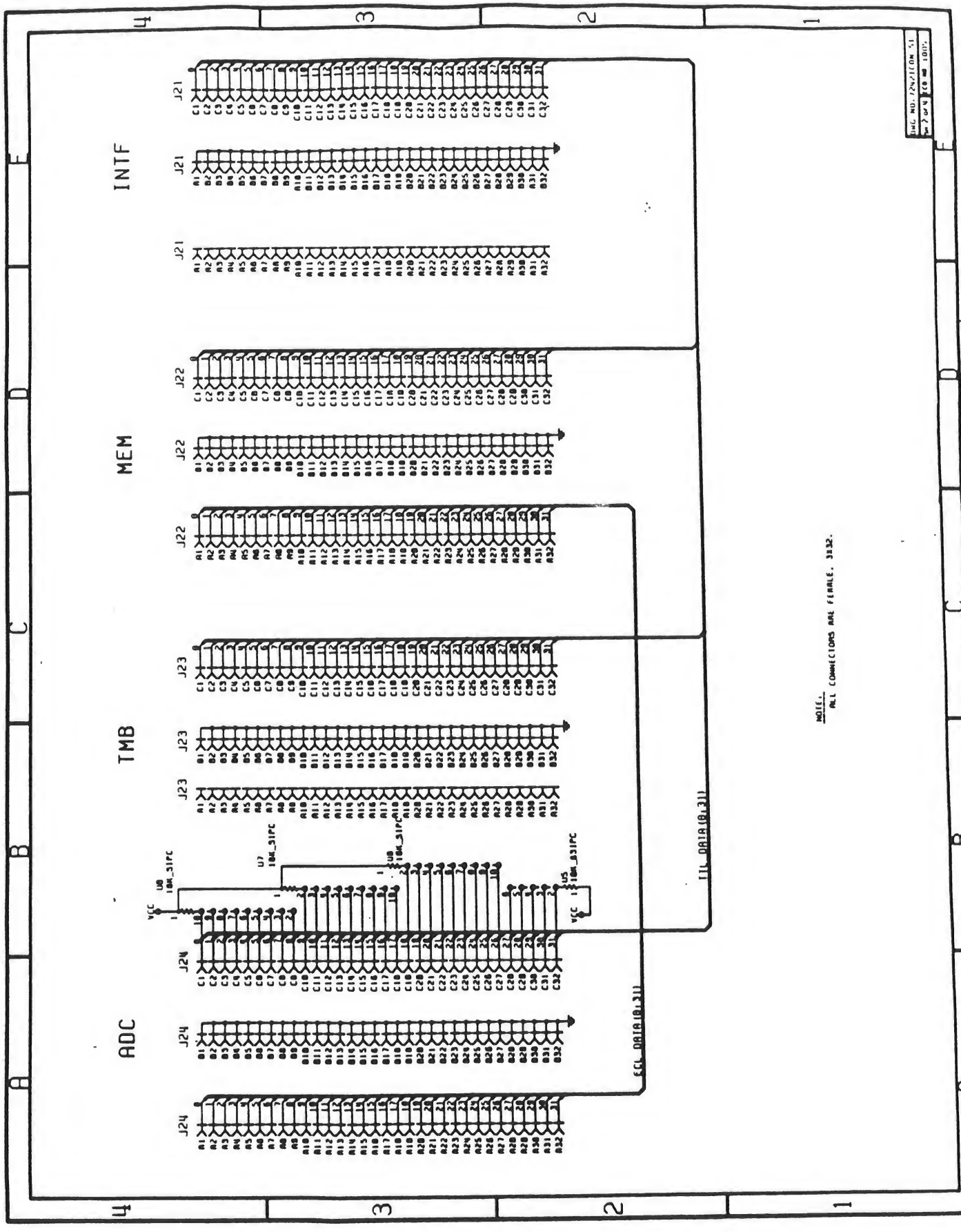

7242EXTR



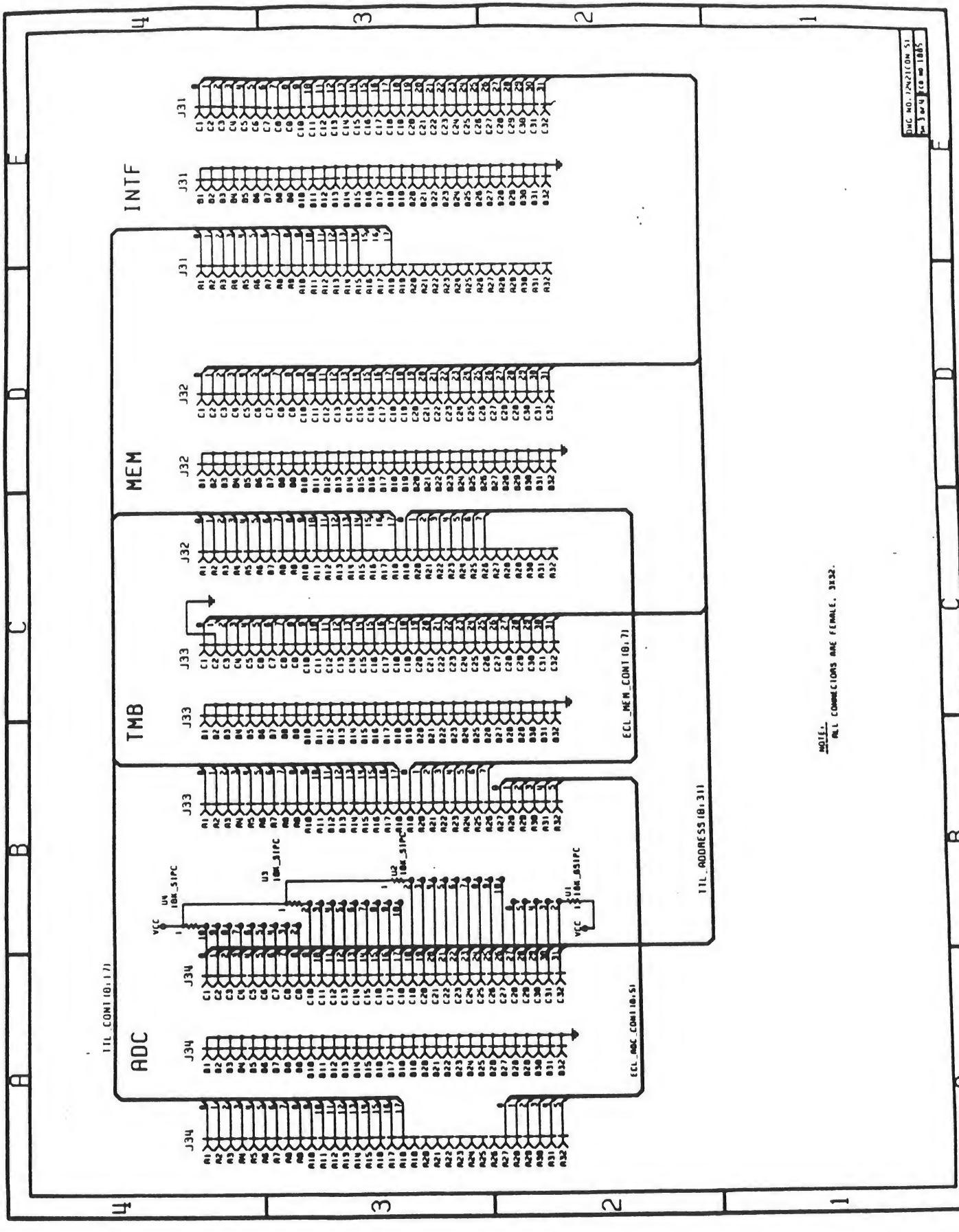




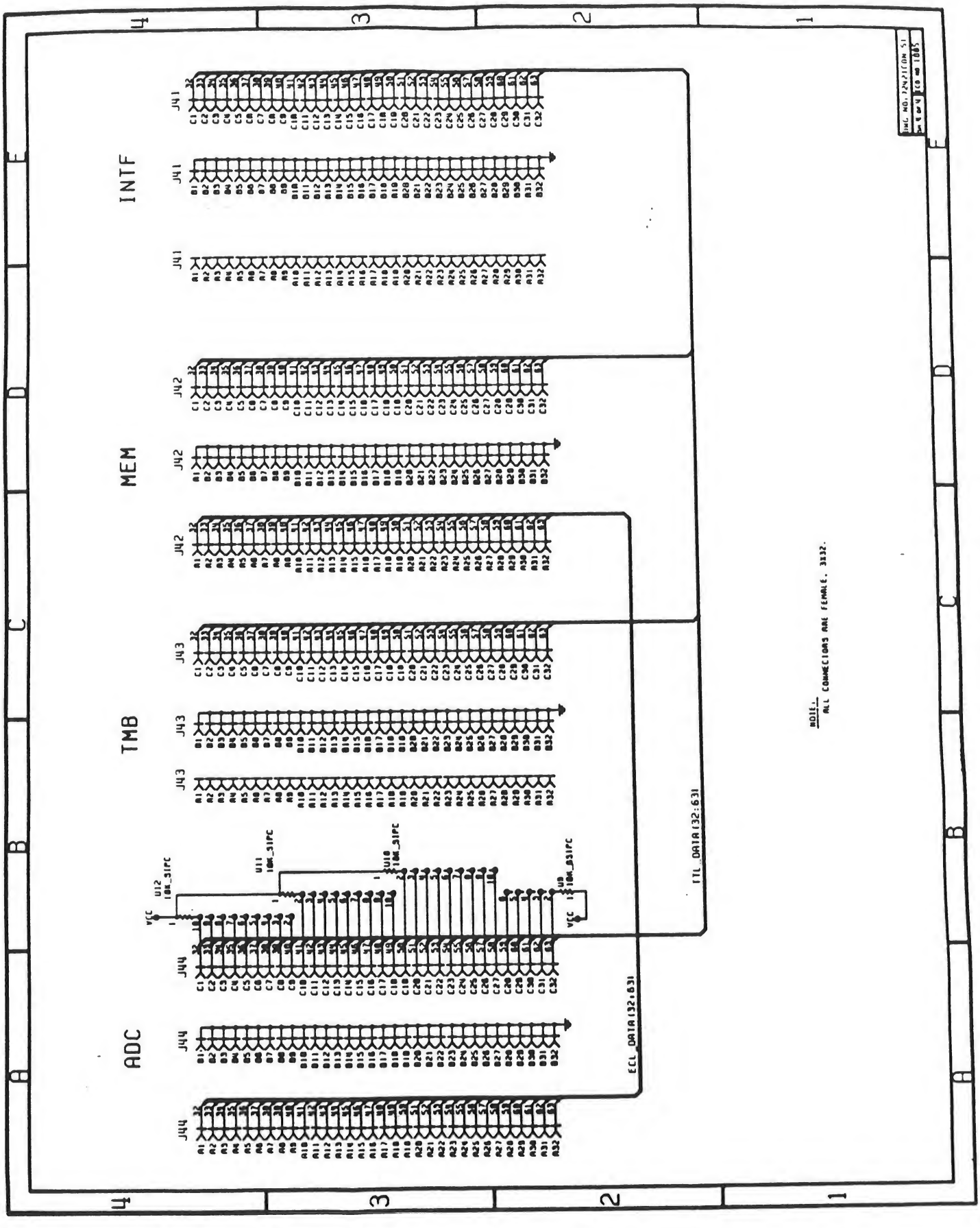
7242ICON **Sheet 1.**

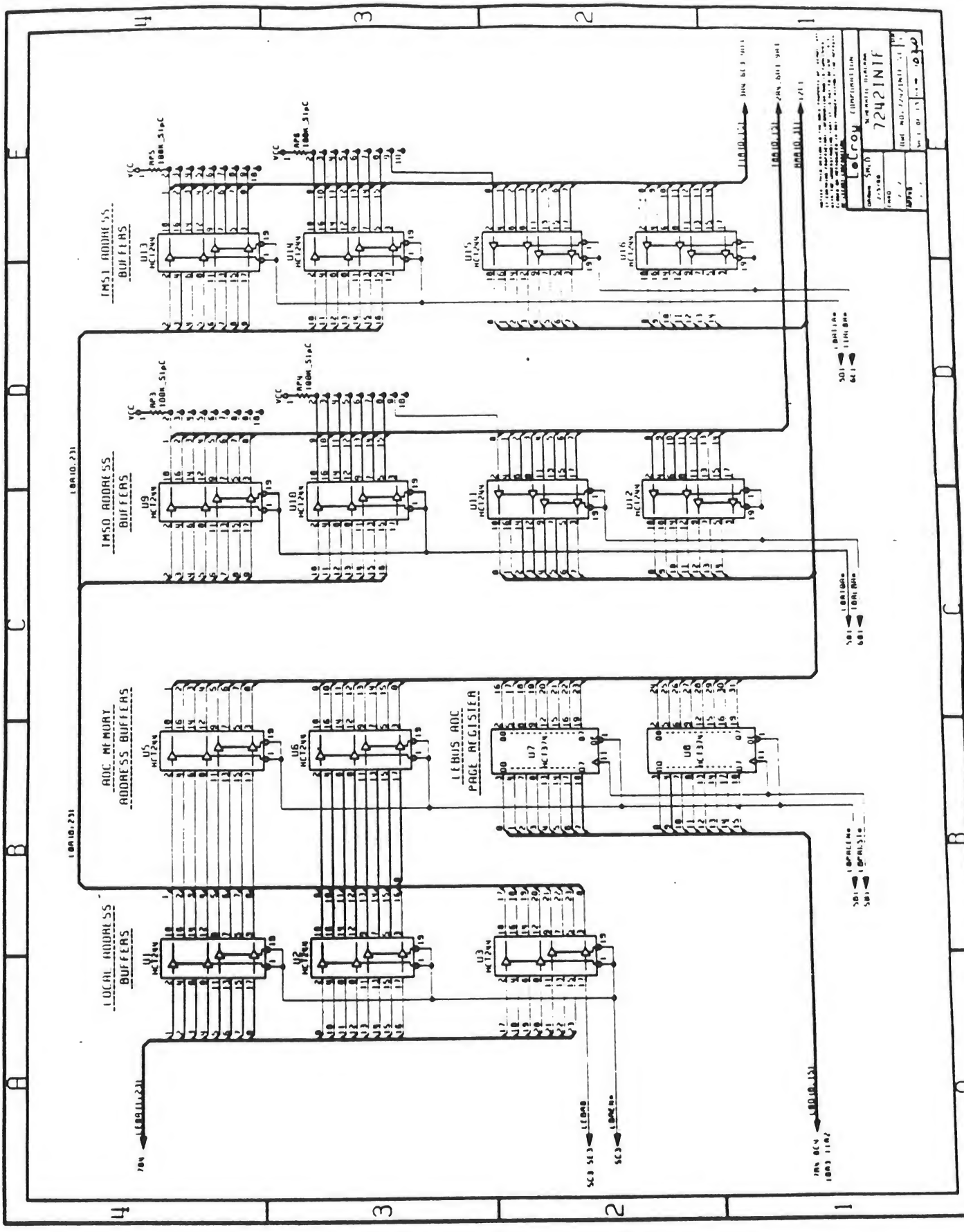


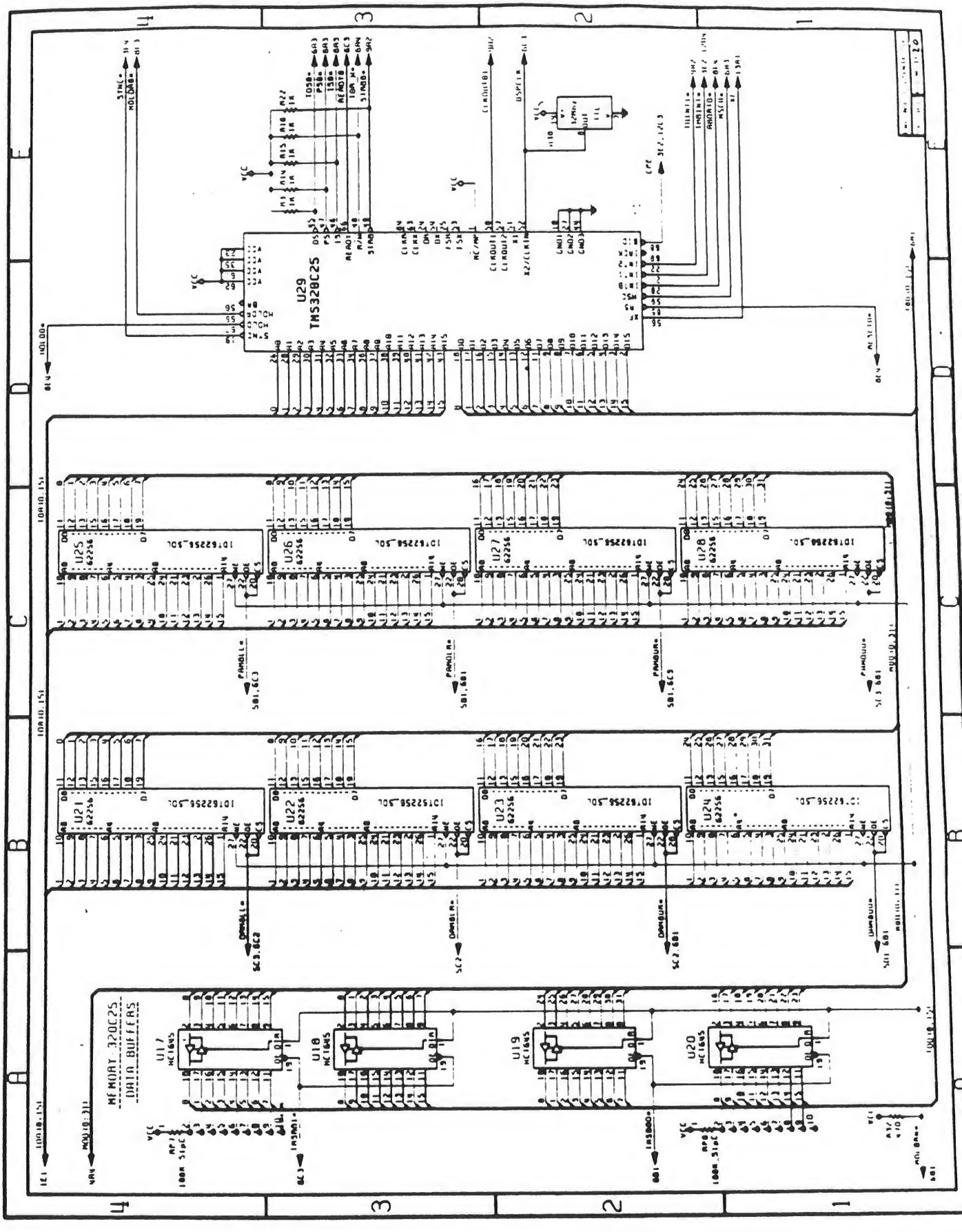
7242ICON **Sheet 2.**



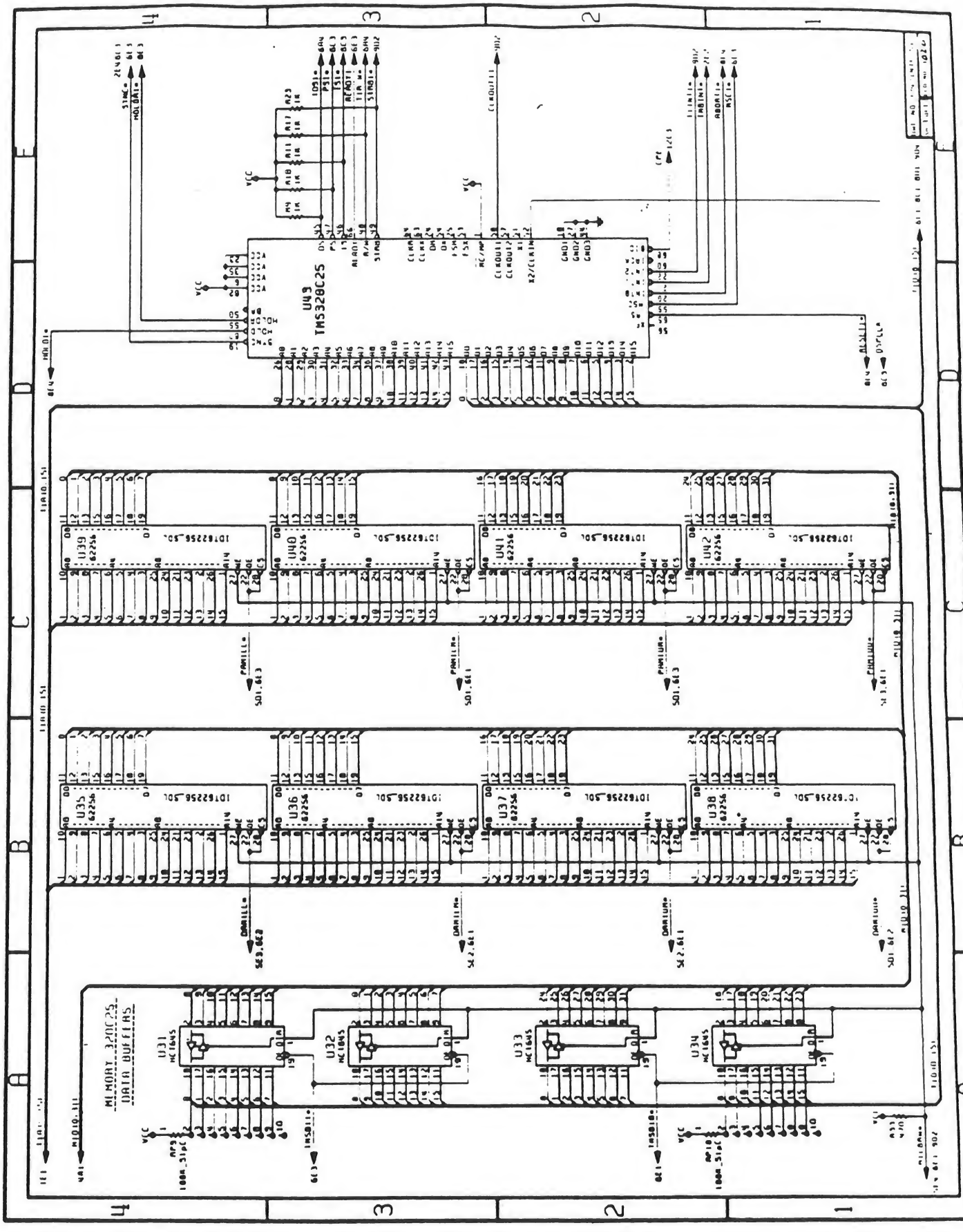
7242ICON **Sheet 3.**

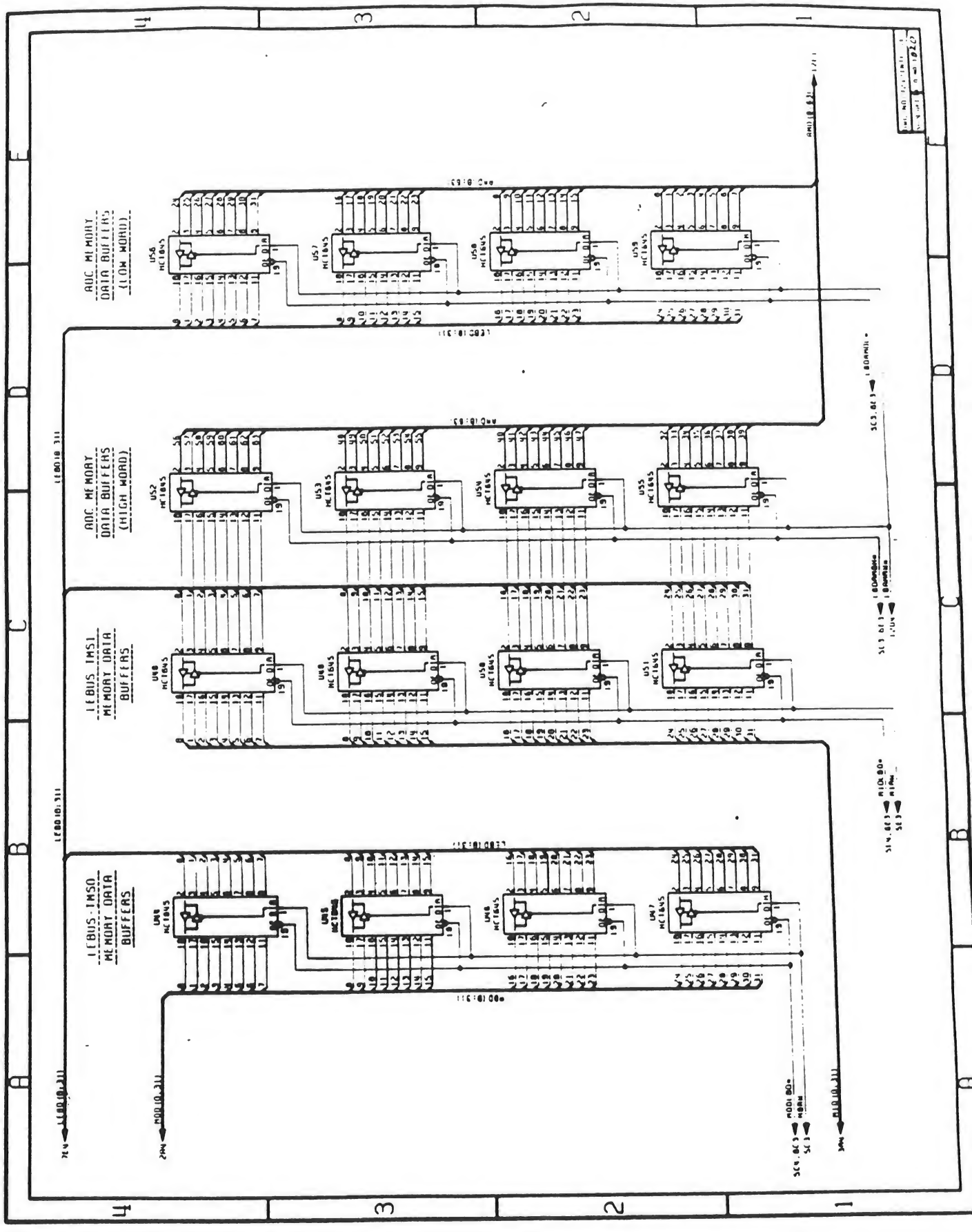

INTF
MEM
TMB
ADC
J41
J42
J43
J44
U11
10K_31PC
U12
10K_31PC
U10
10K_31PC
U9
10K_31PC
VCC
TTL_DATA(32:63)
ECL_DATA(32:63)
NOTE:
ALL CONNECTORS ARE FEMALE, 3332.


IMS1 ADDRESS BUFFERS
IMS0 ADDRESS BUFFERS
ADC MEMORY ADDRESS BUFFERS
LOCAL ADDRESS BUFFERS
LEBUS ADC PAGE REGISTER
7242INTF

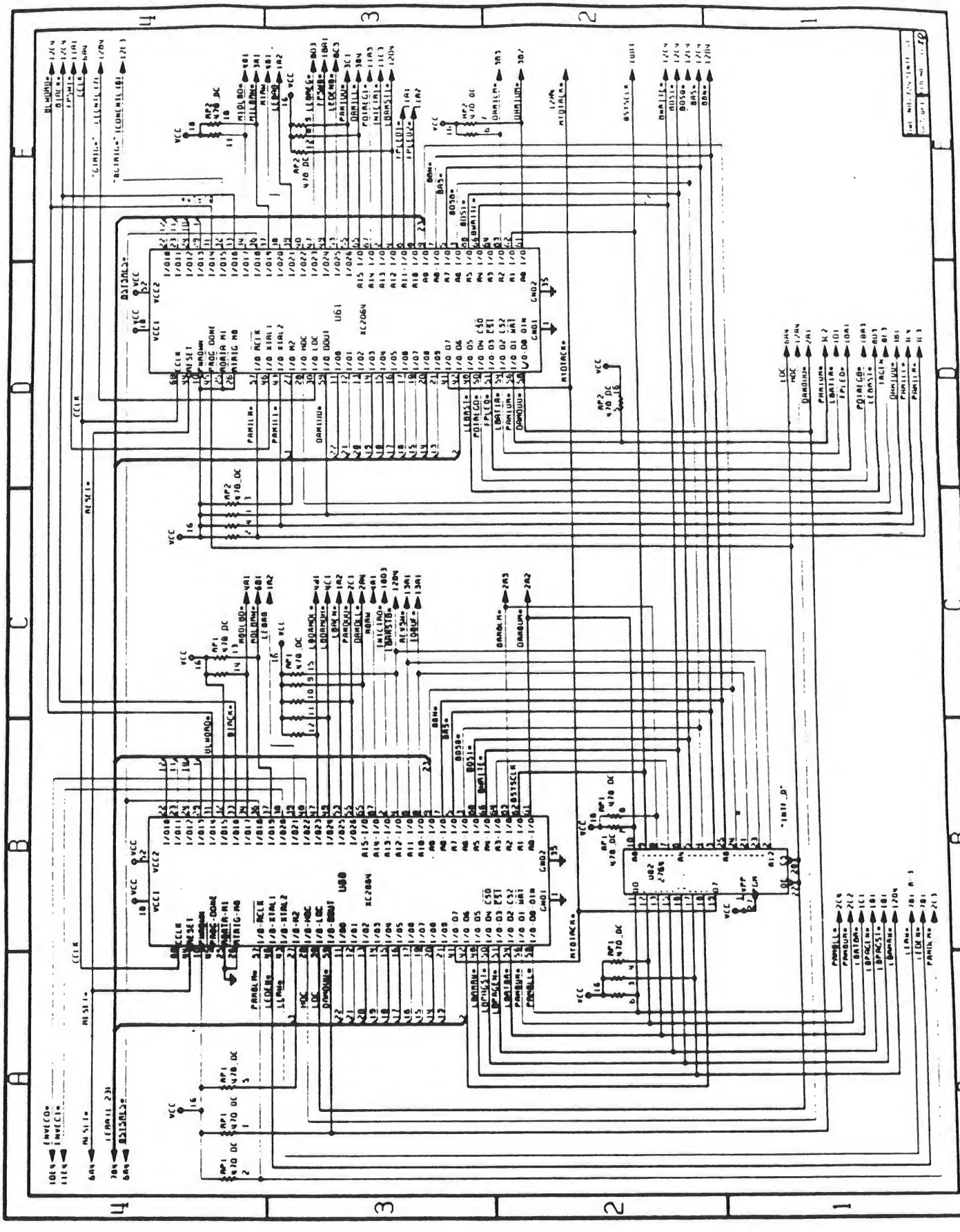


7242INTF **Sheet 2.**

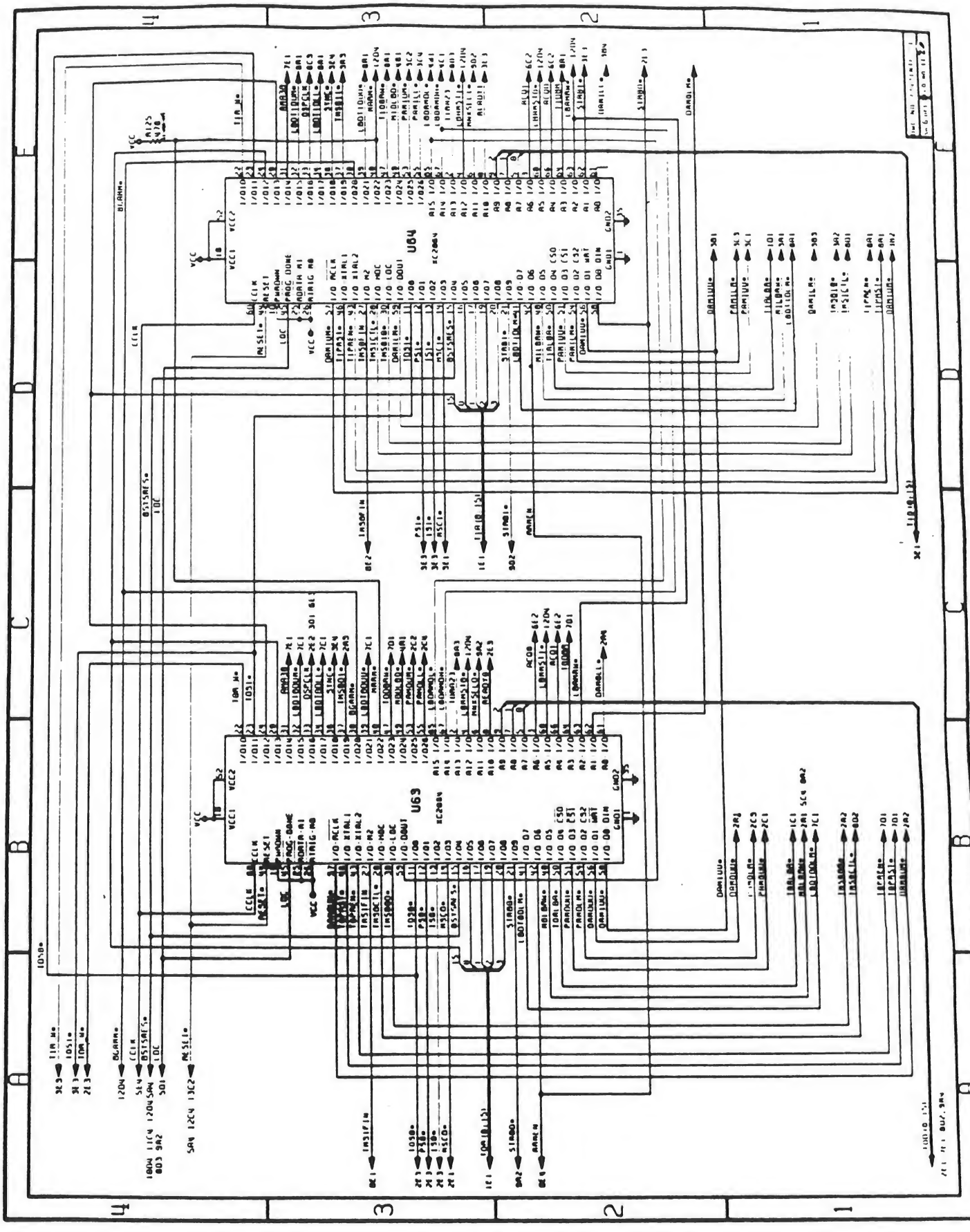

U43
TMS320C25
MEMORY 320C25
DATA BUFFERS
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
U41
U42



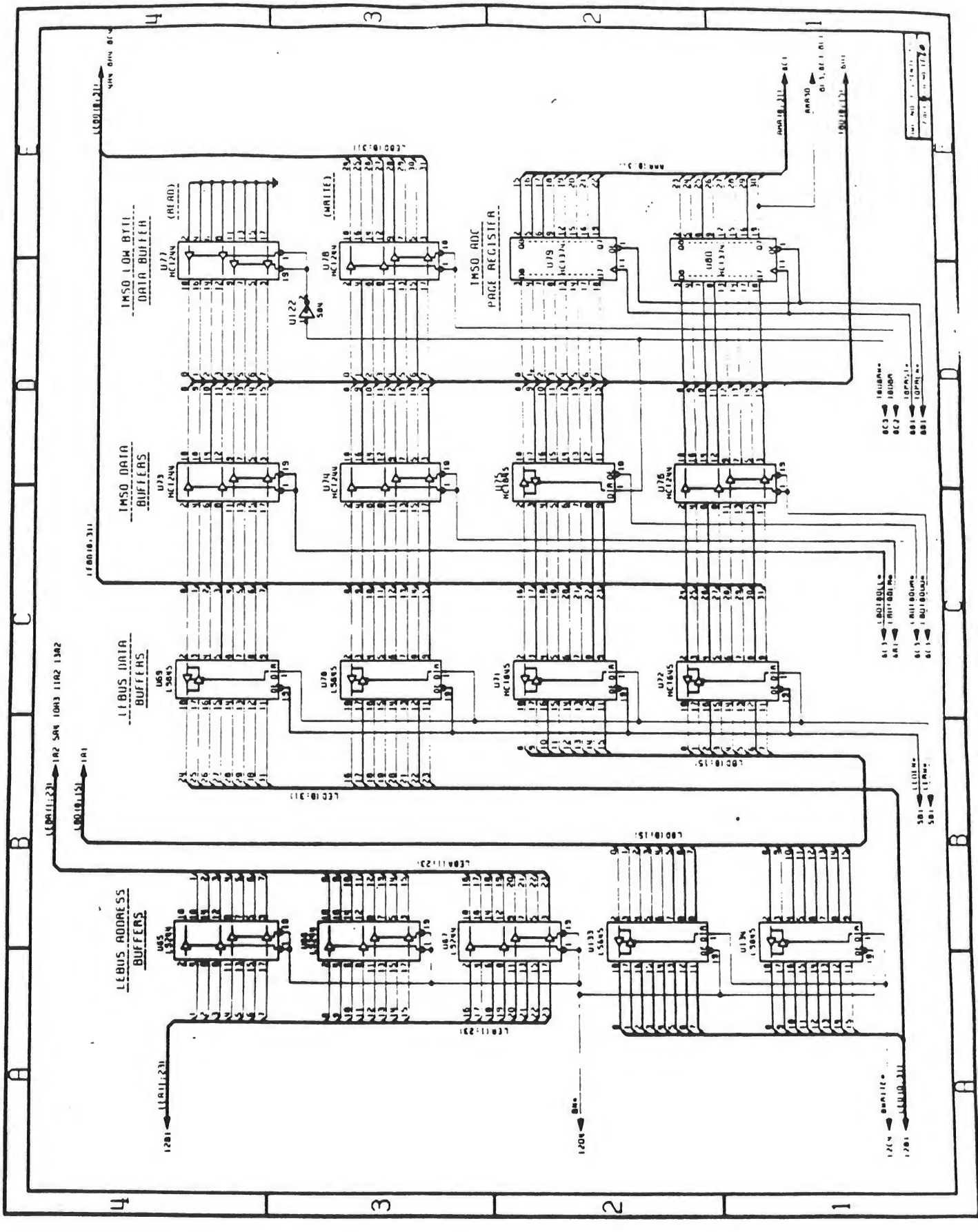
7242INTF **Sheet 4.**



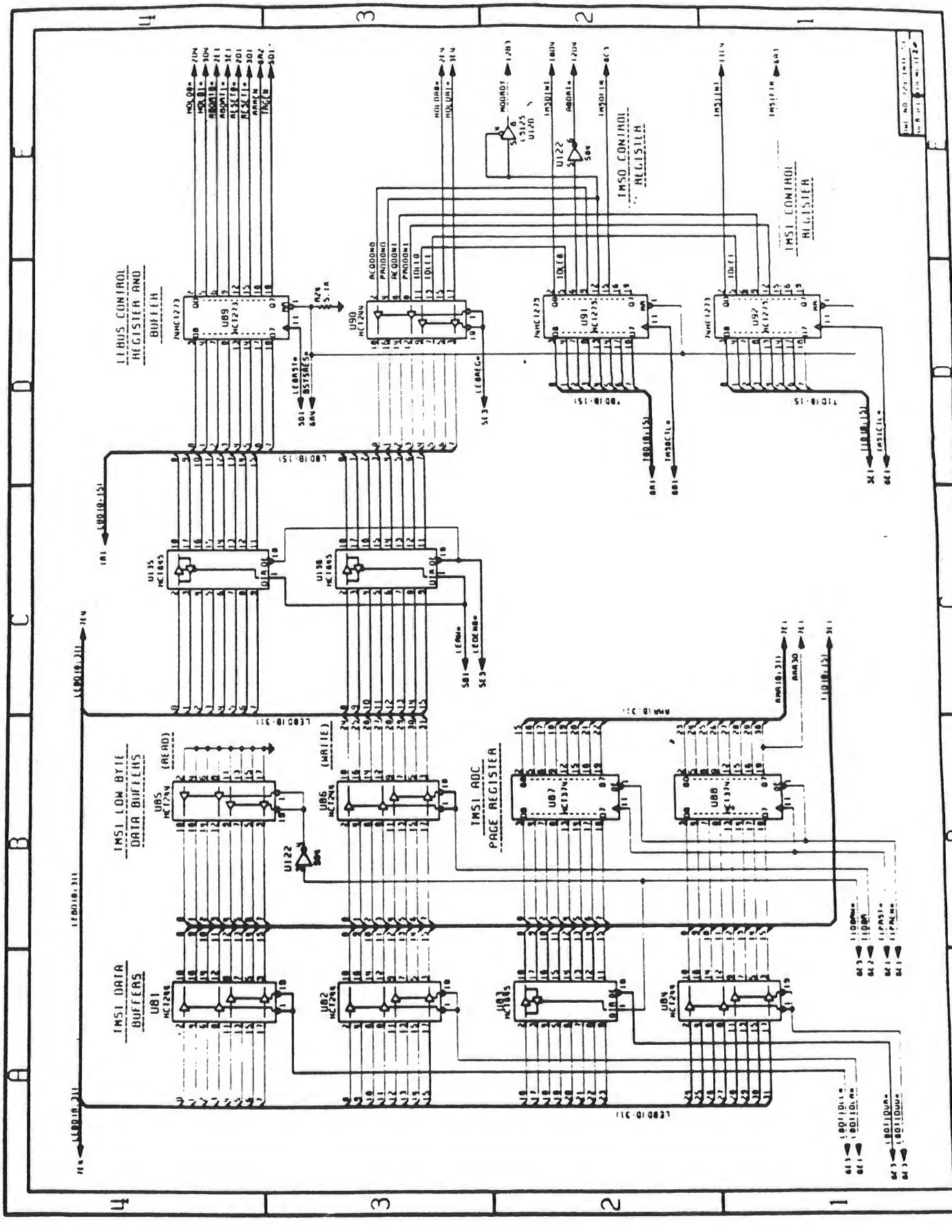
7242INTF **Sheet 5.**



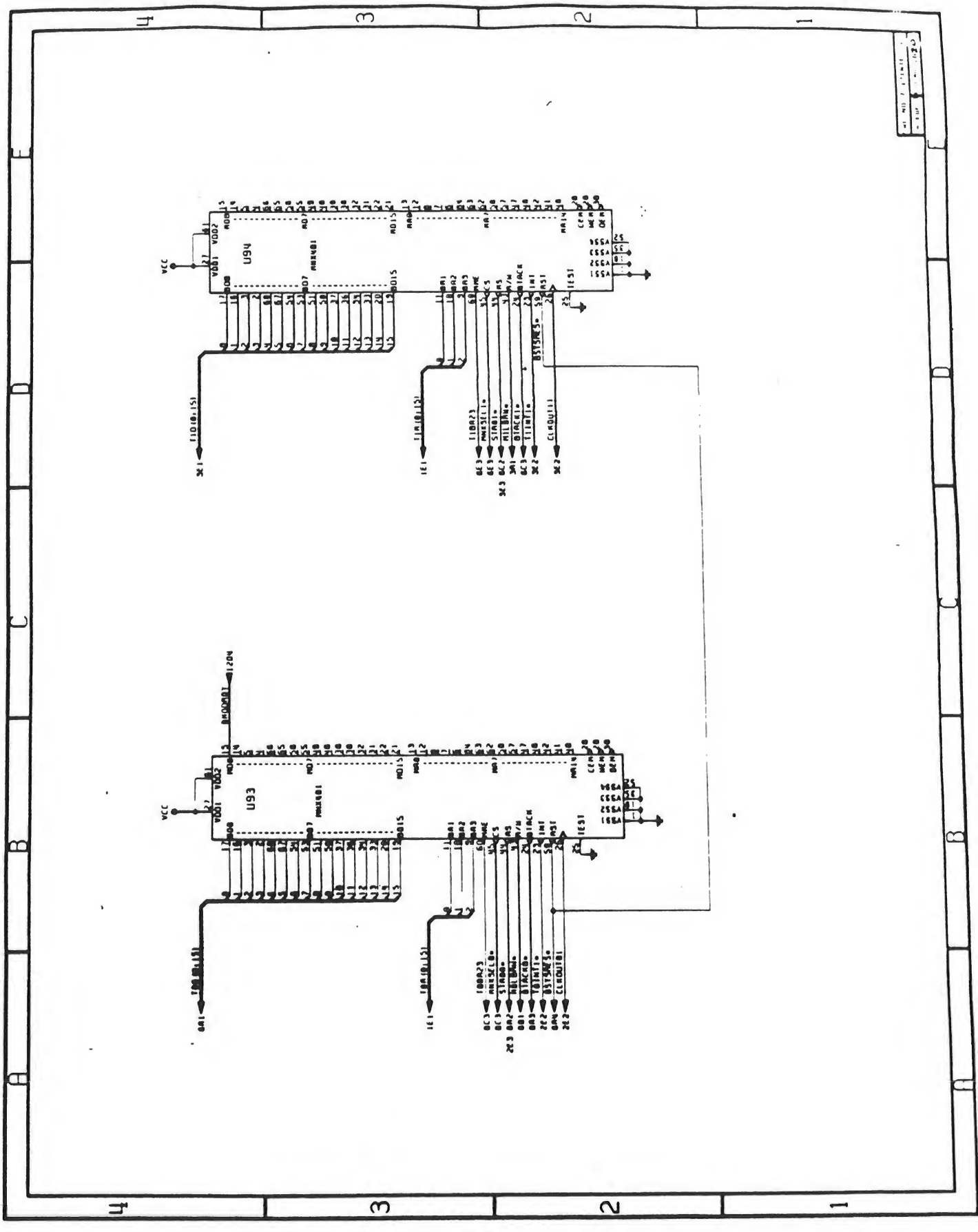
7242INTF **Sheet 6.**

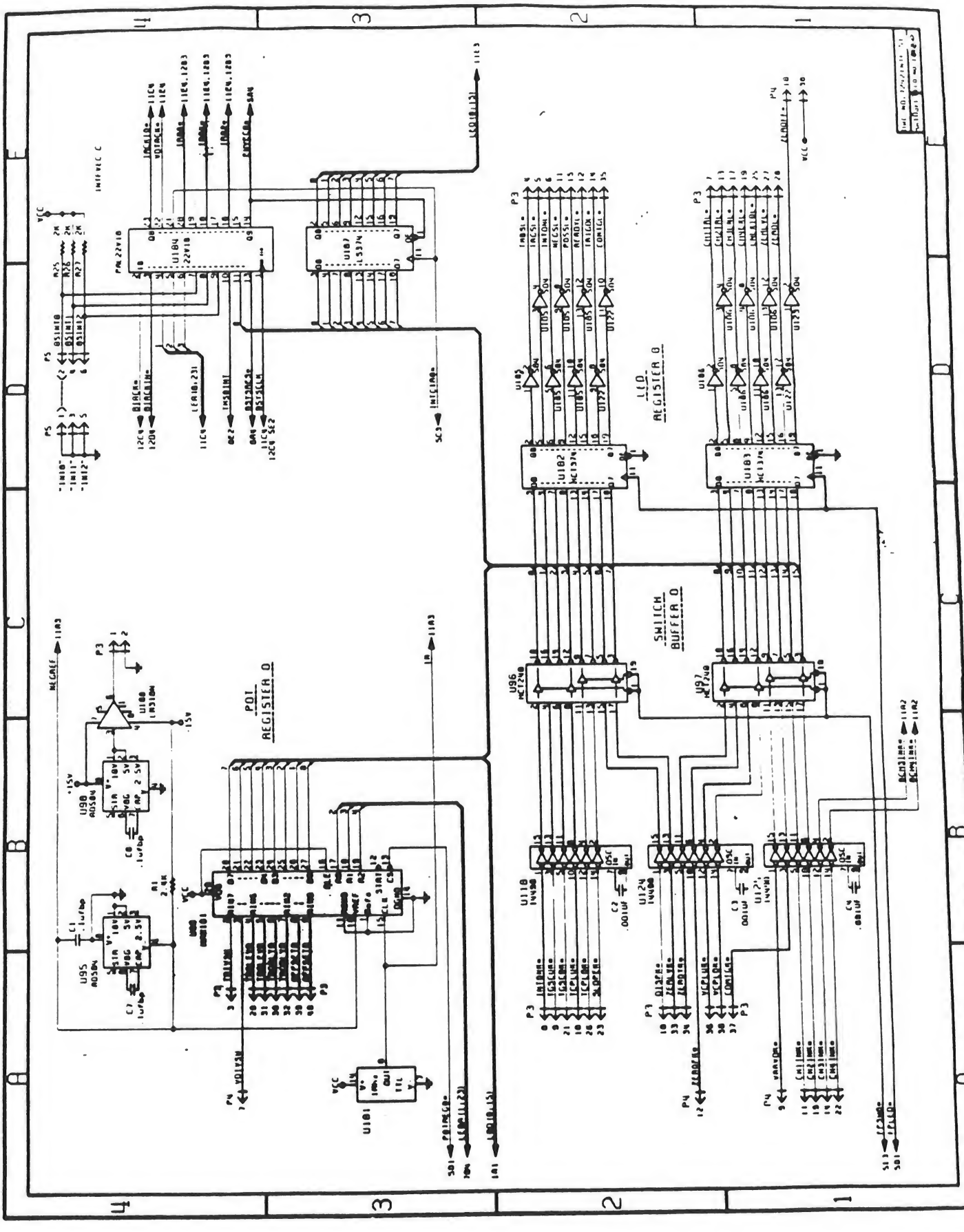


7242INTF **Sheet 7.**

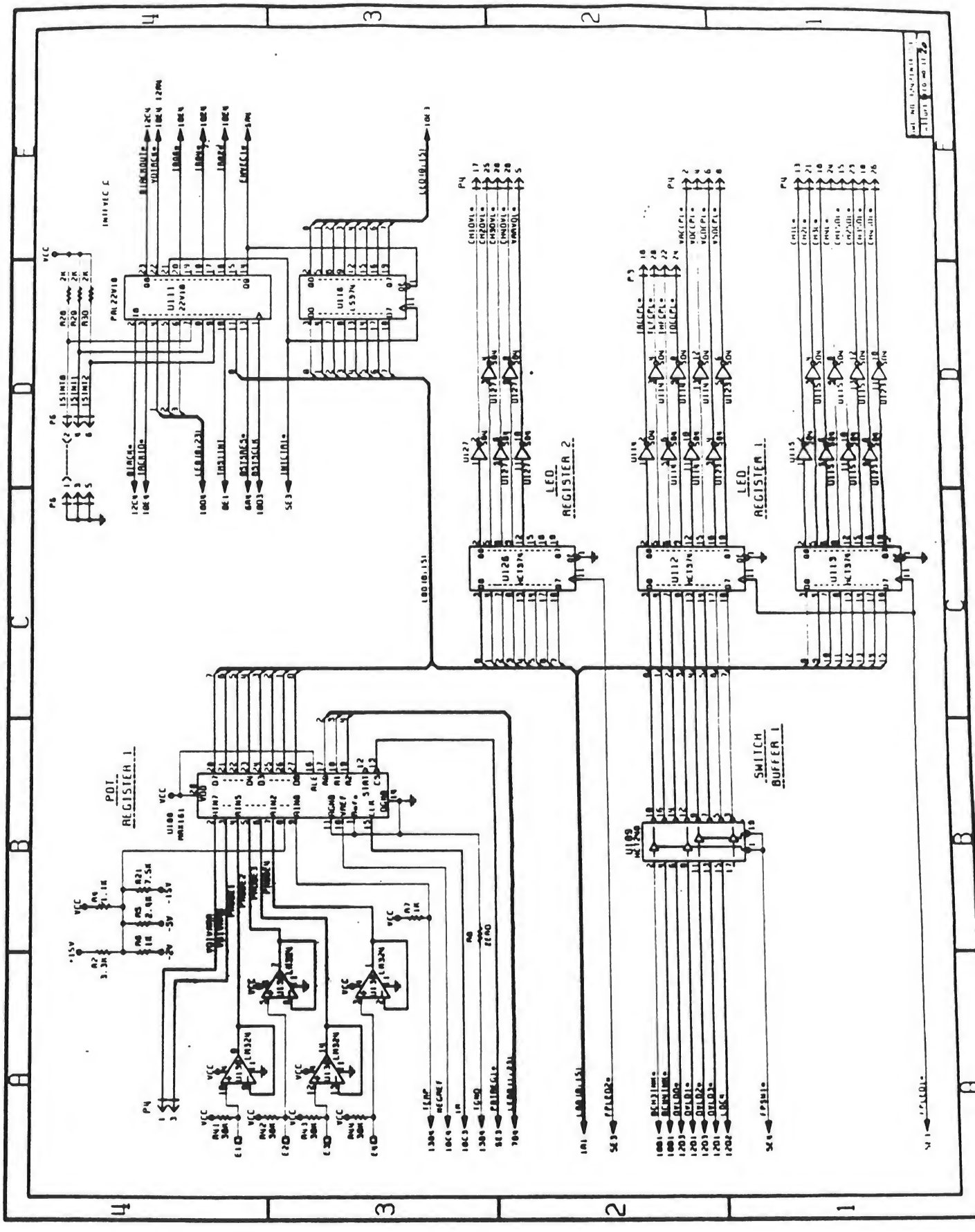


7242INTF **Sheet 8.**

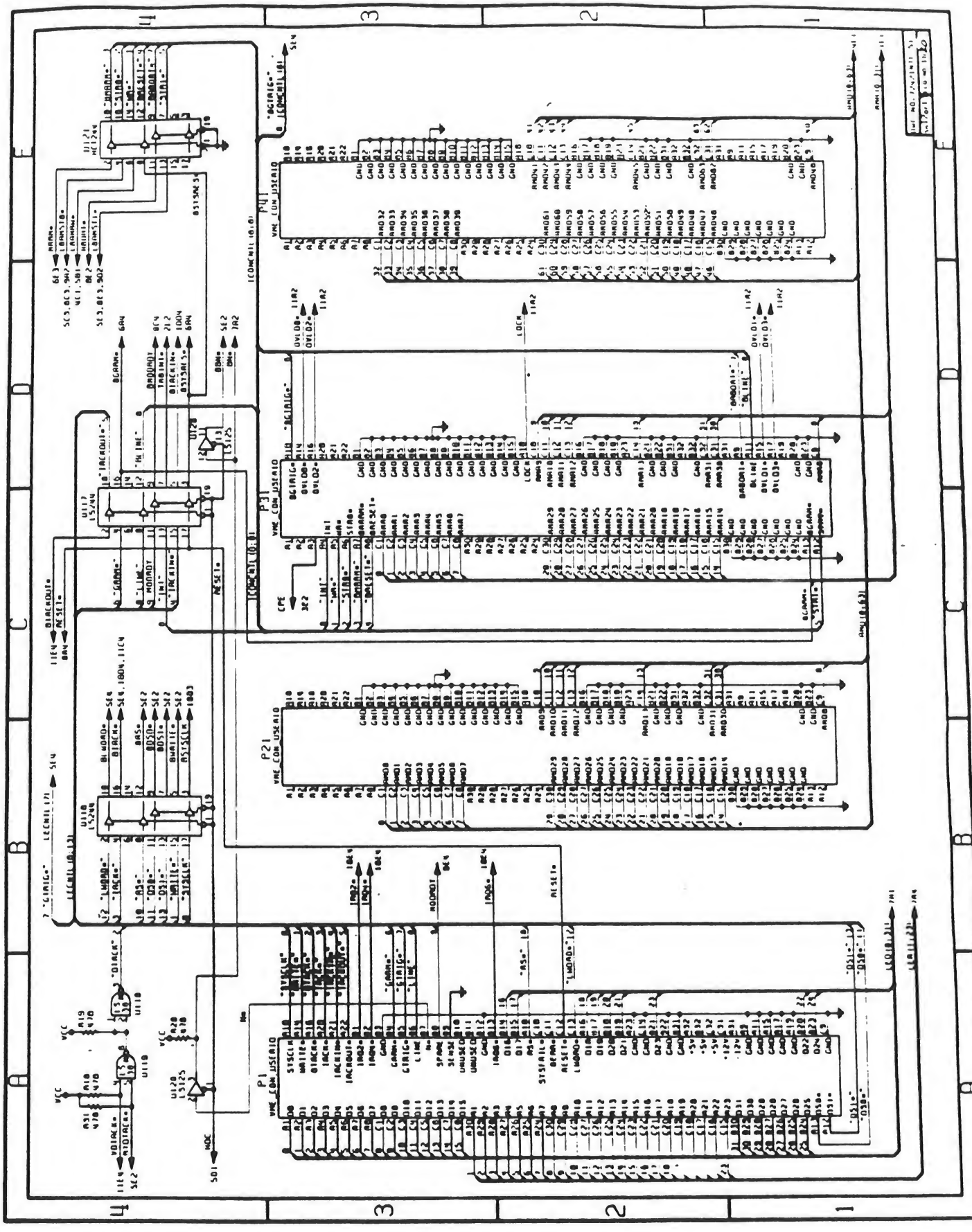




7242INTF **Sheet 10.**



7242INTF **Sheet 11.**



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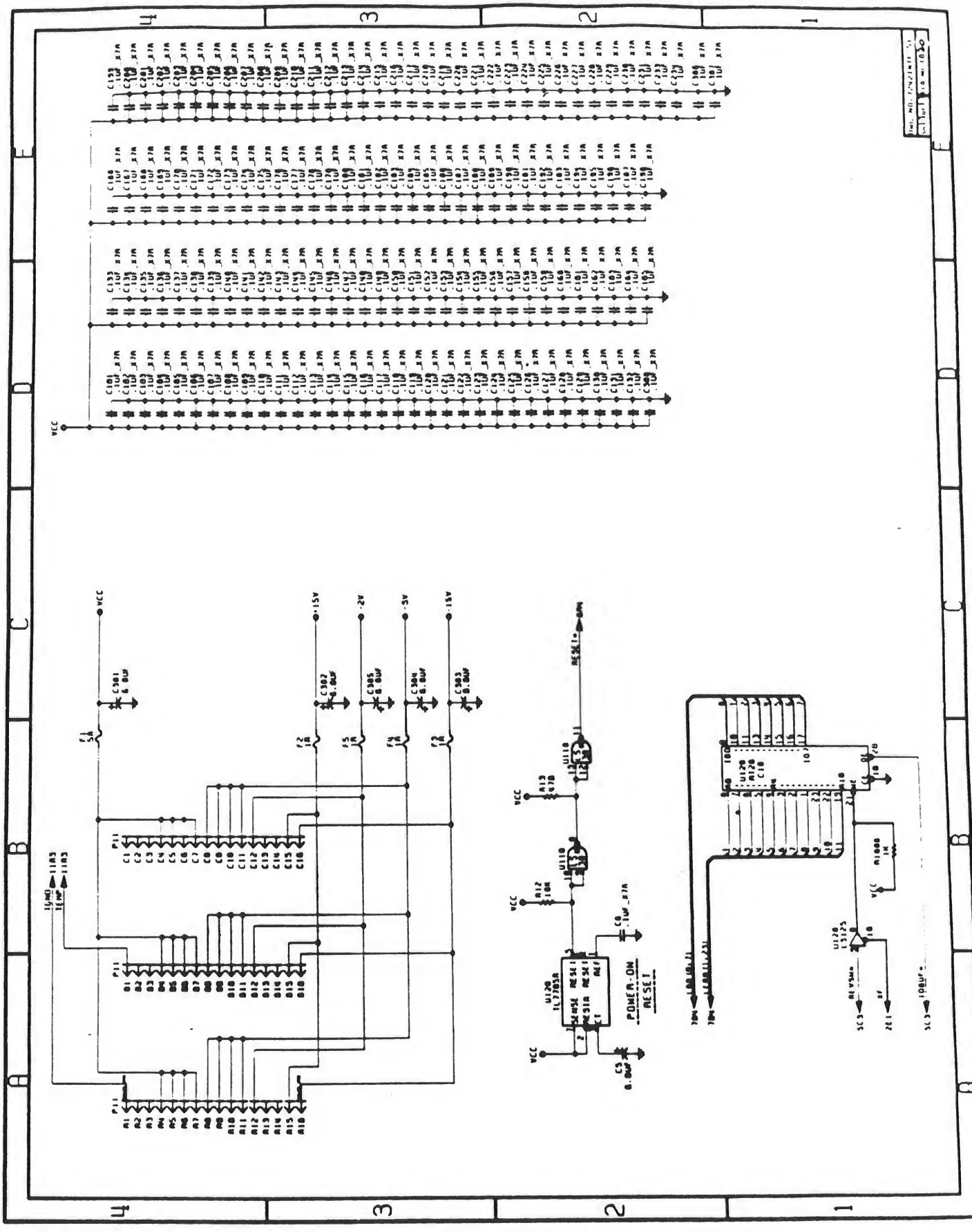

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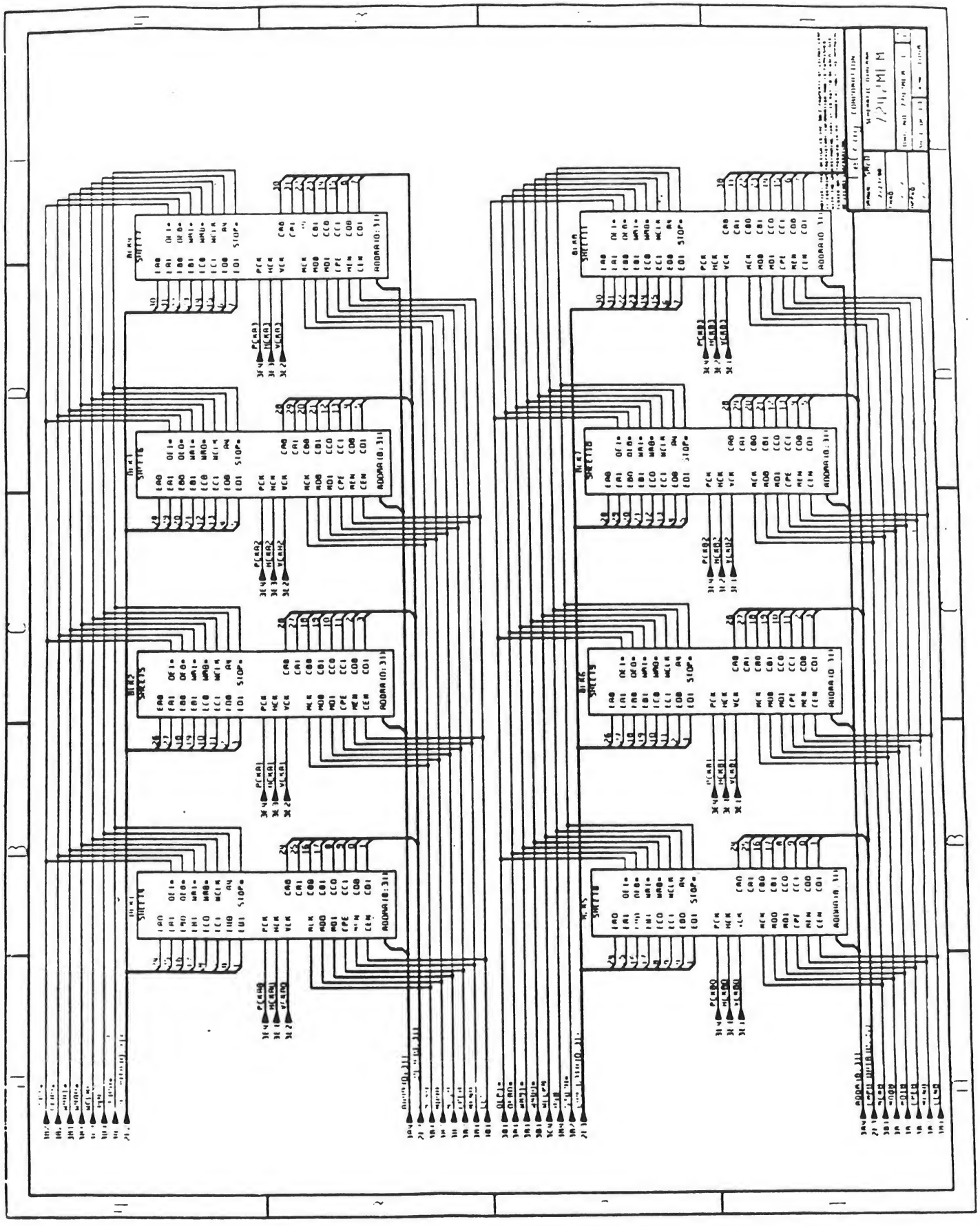

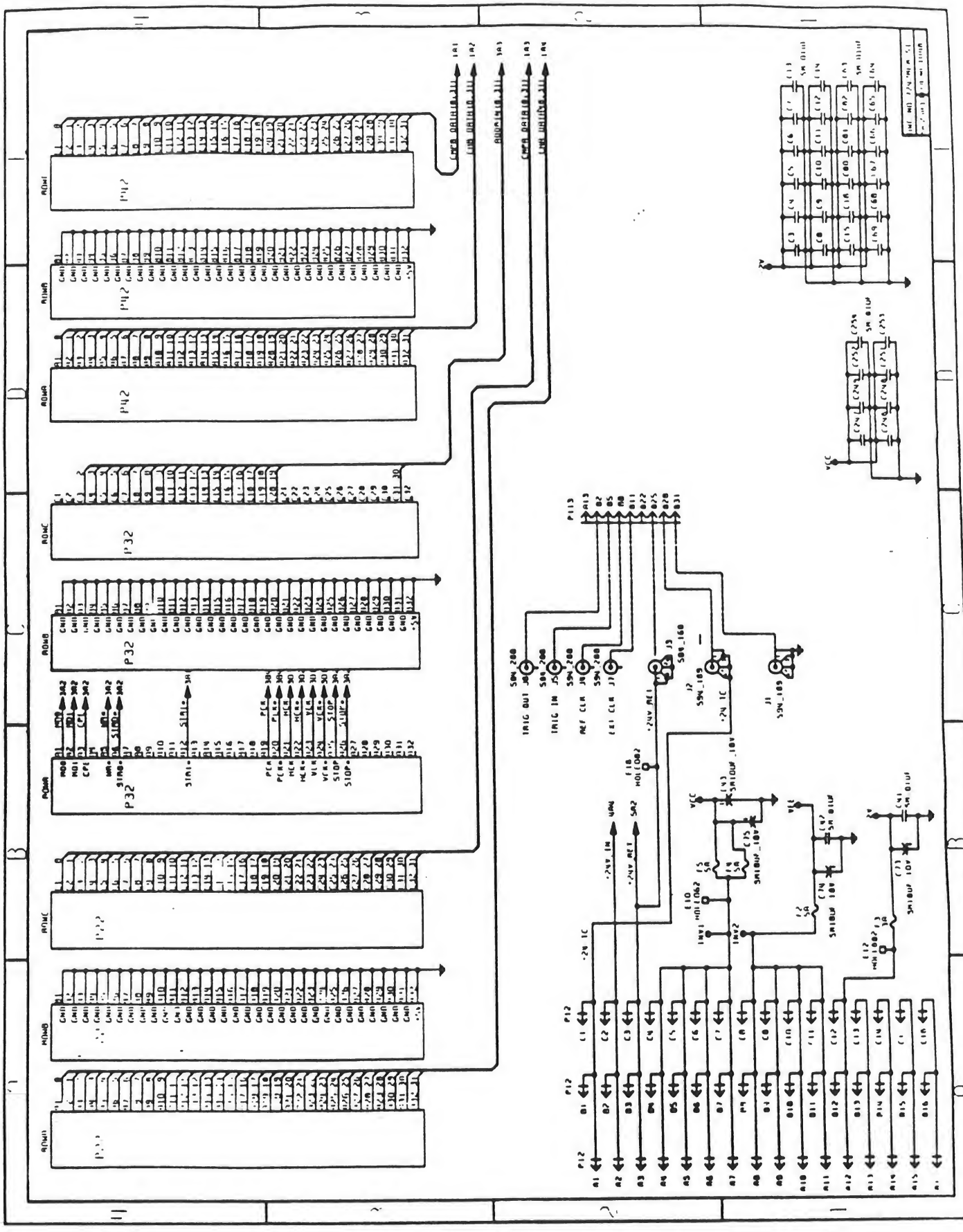

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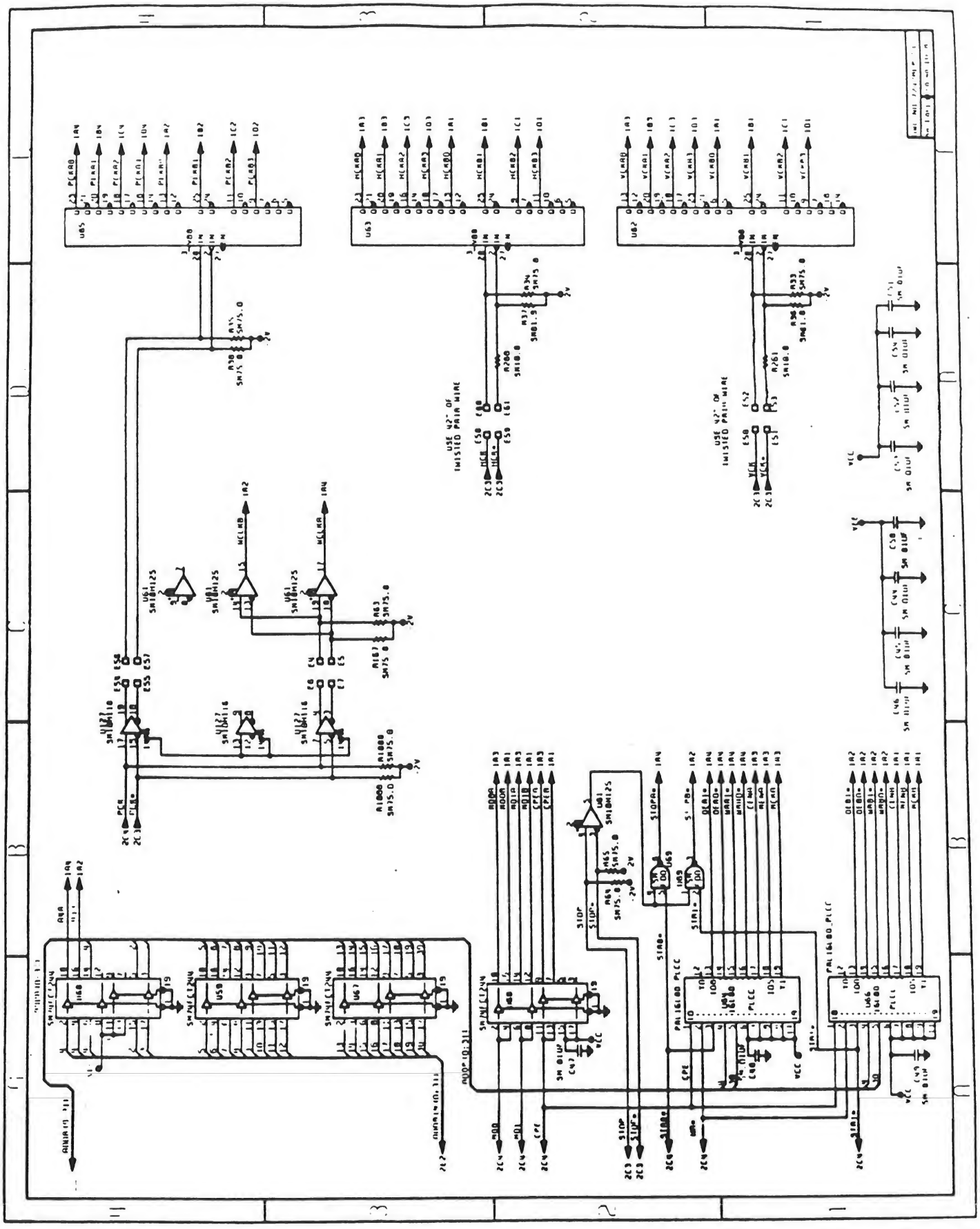

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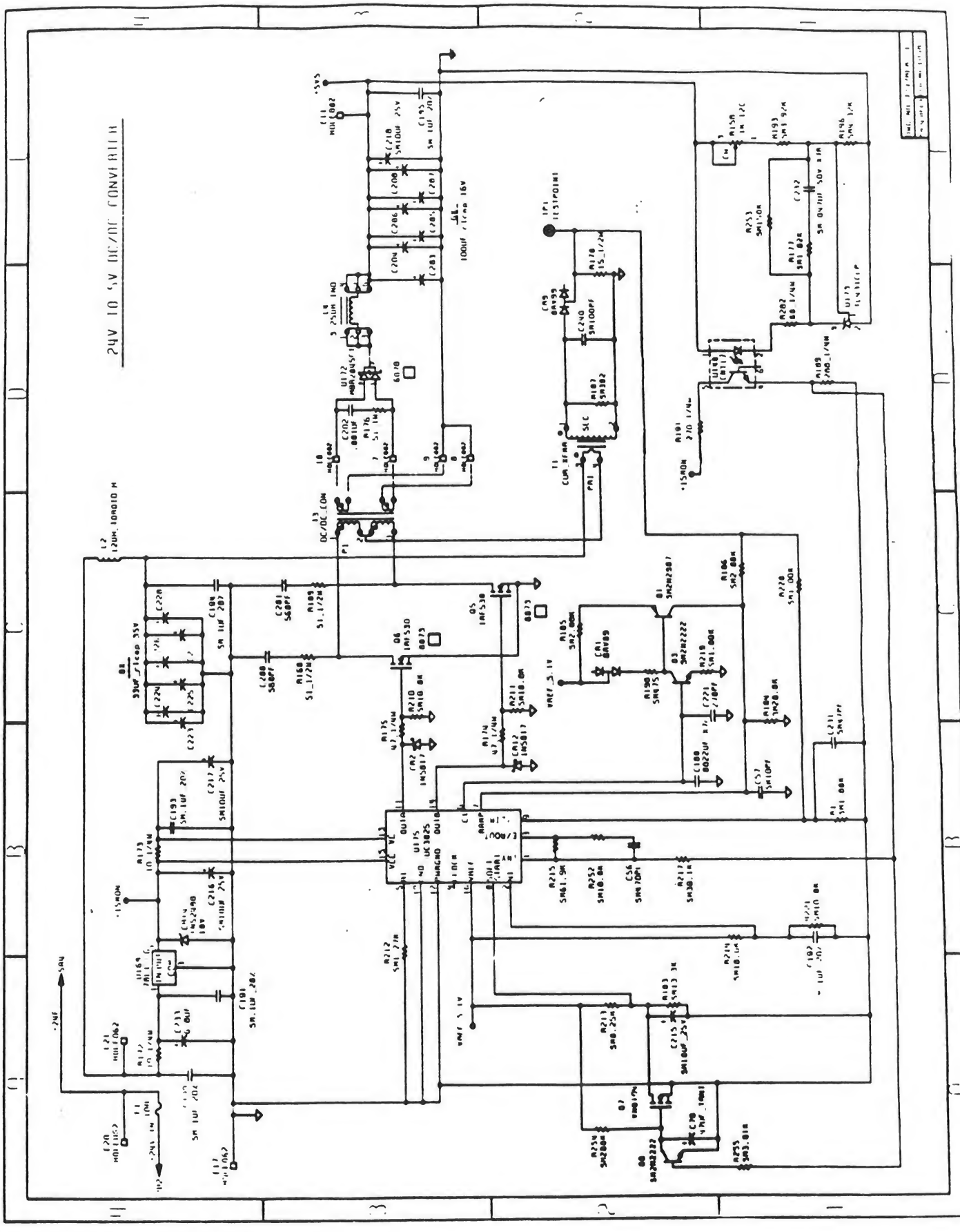

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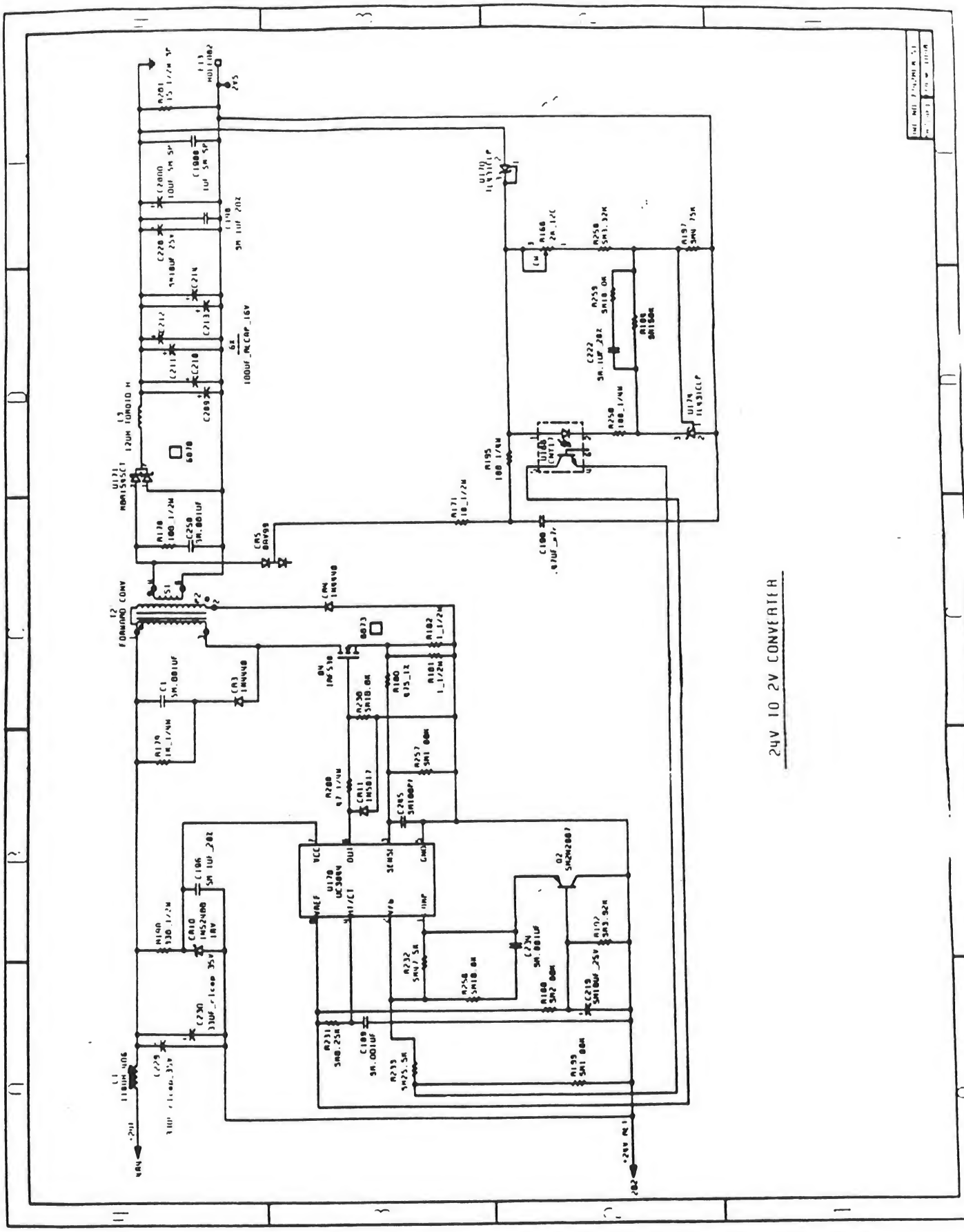

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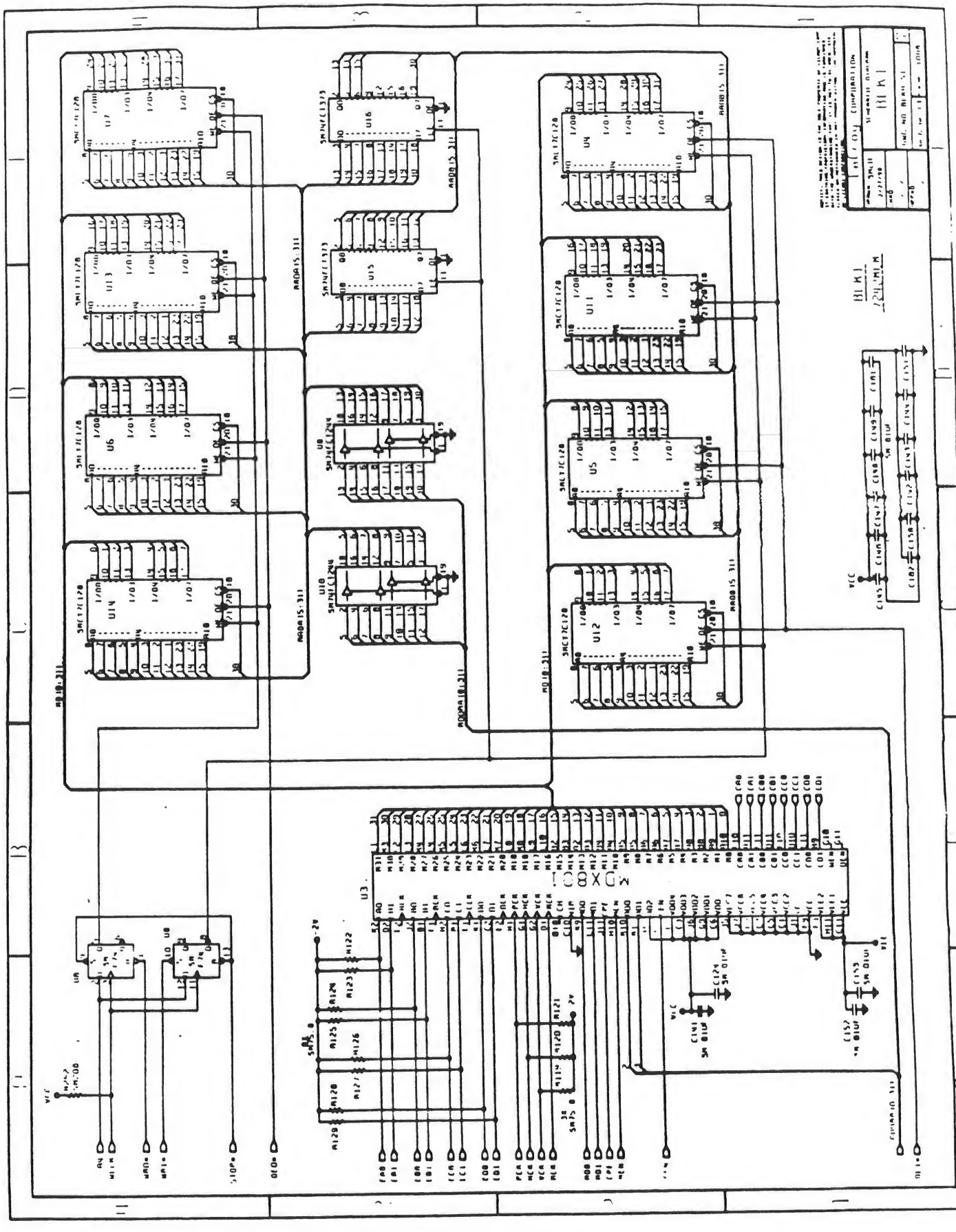

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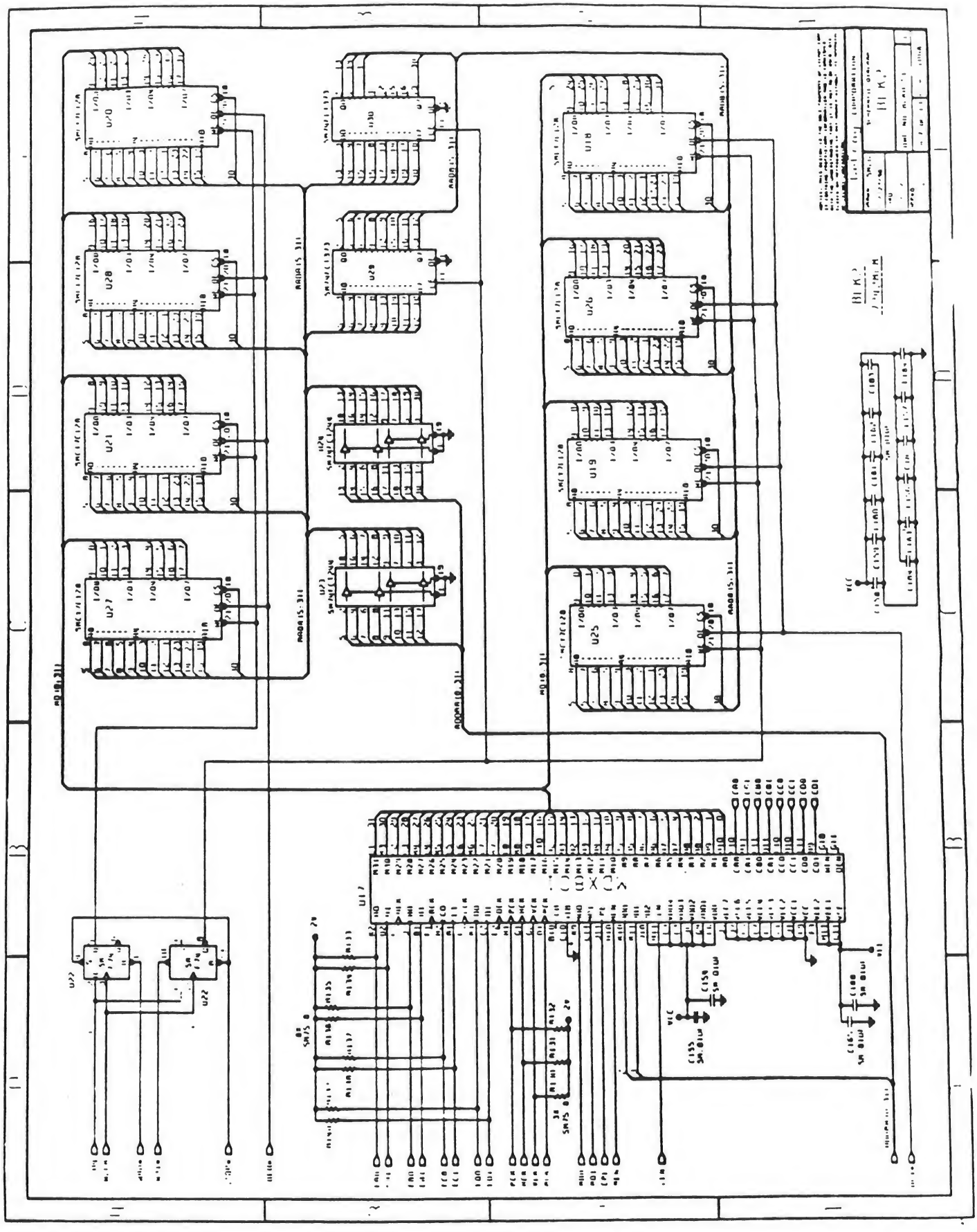

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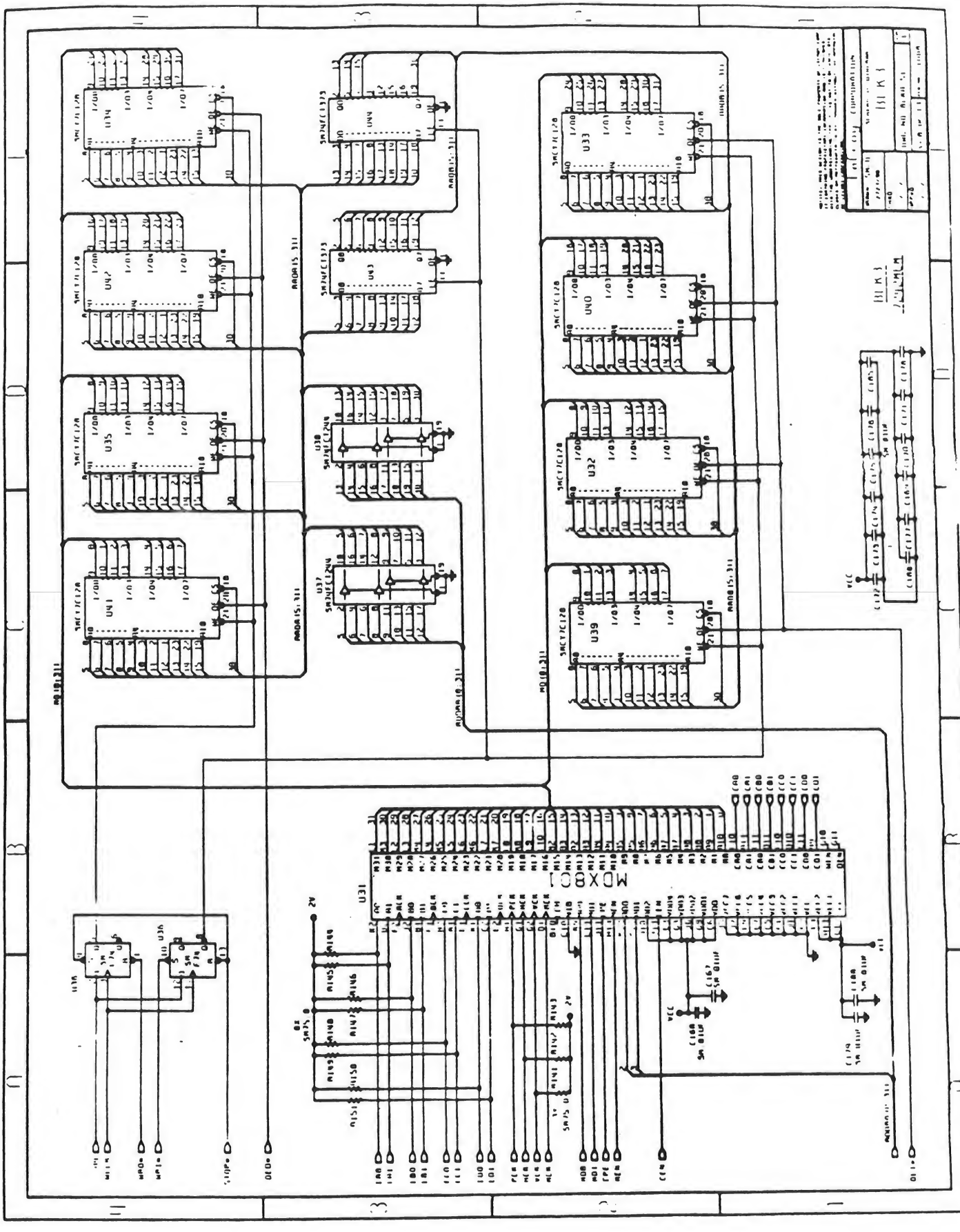

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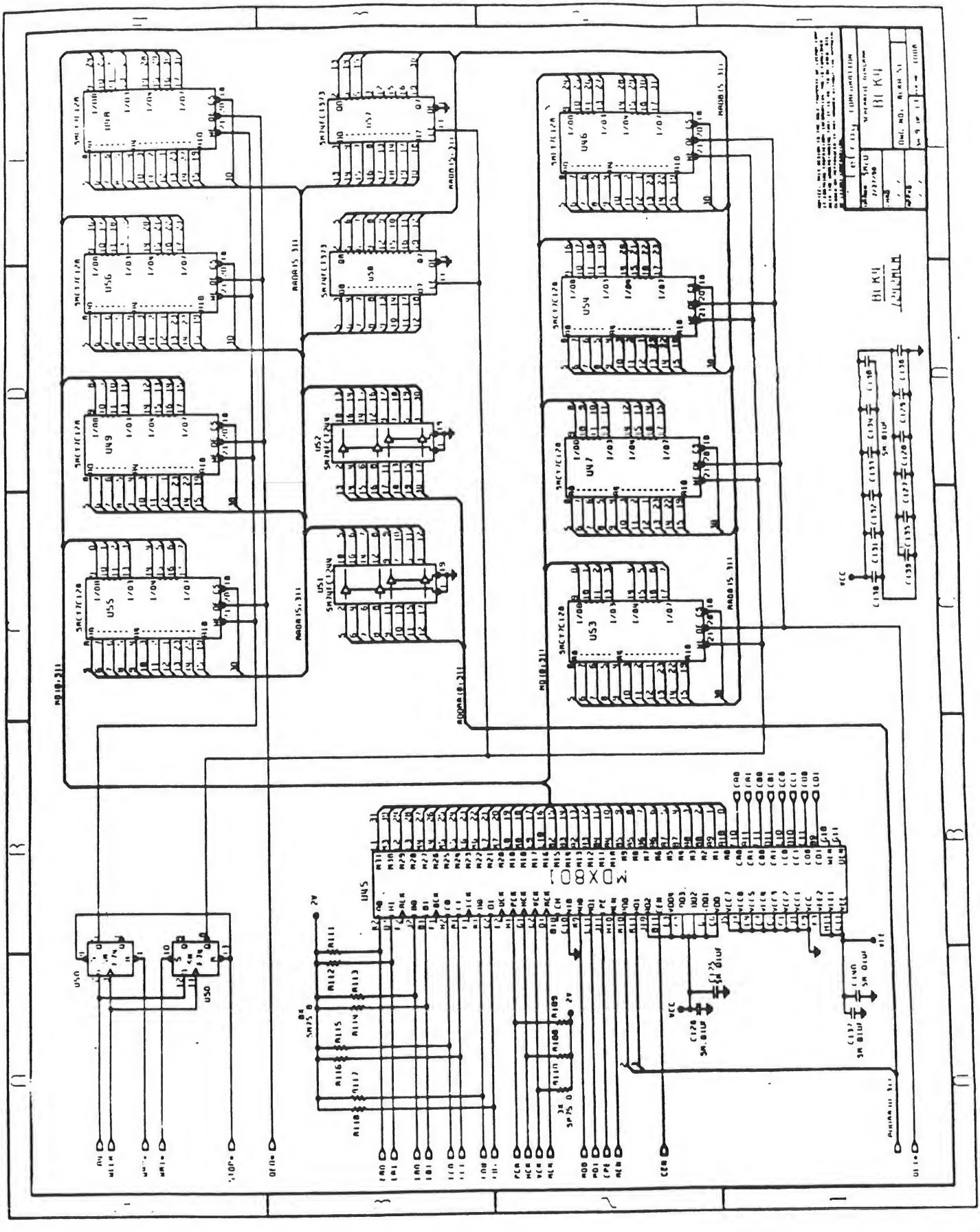

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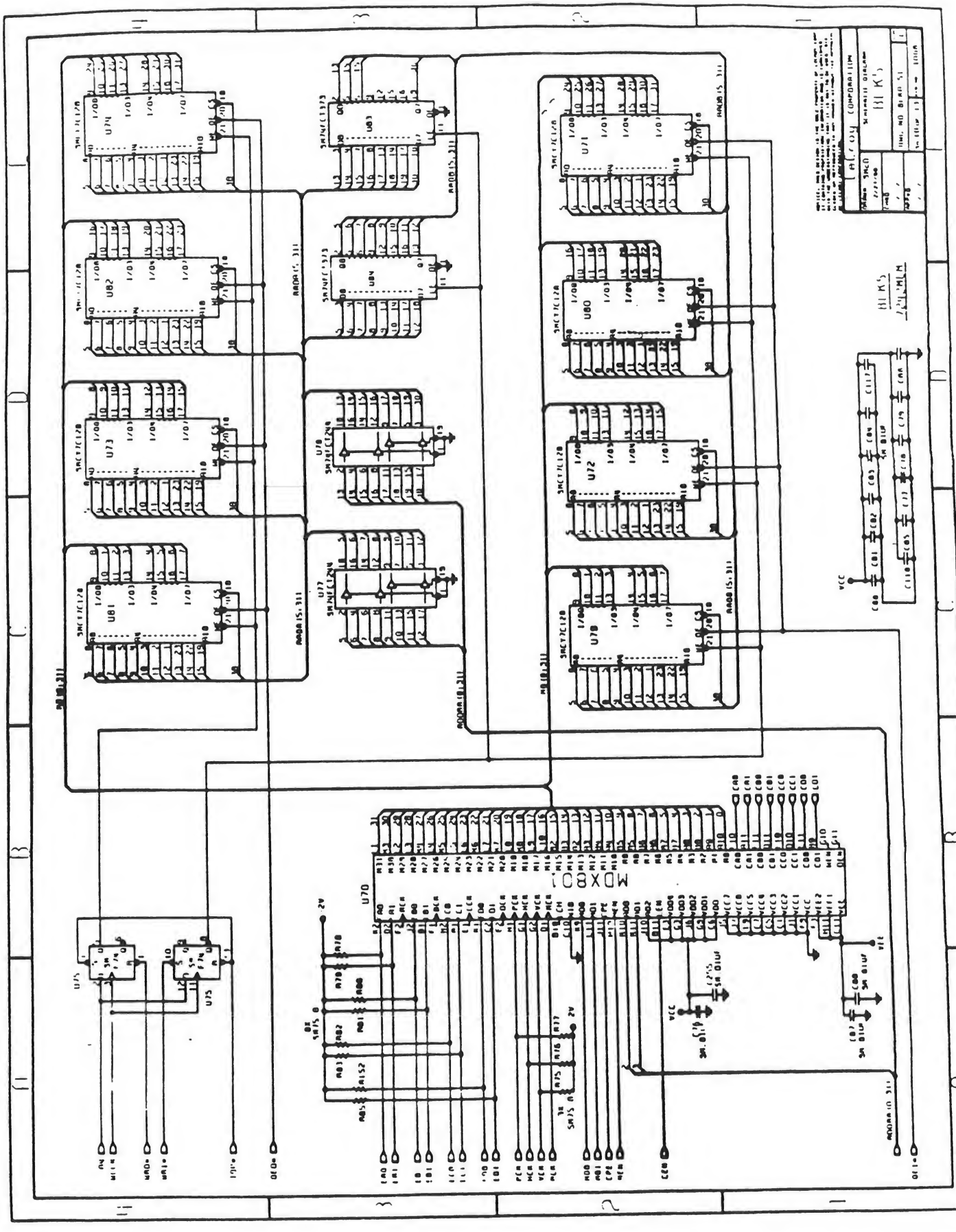

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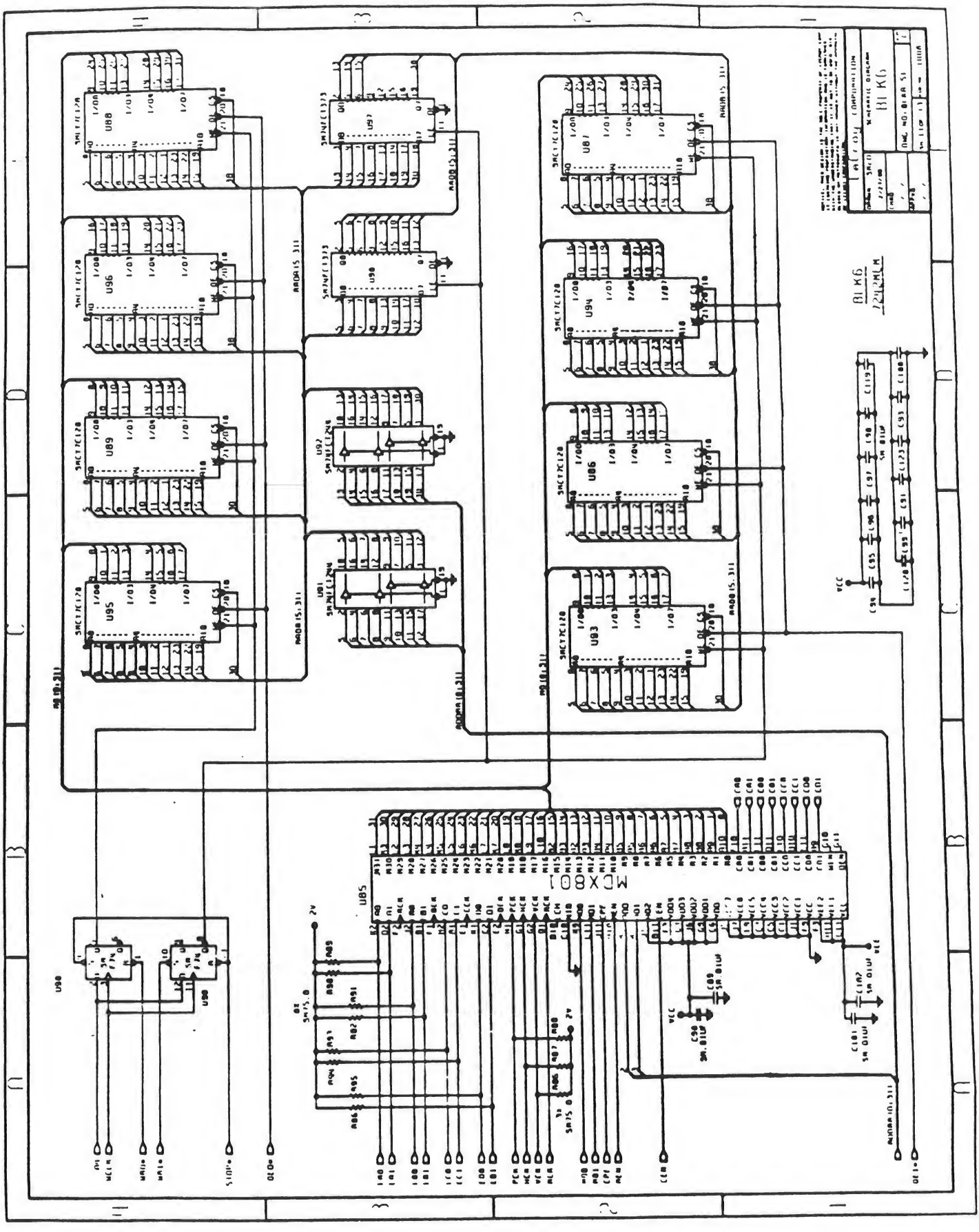

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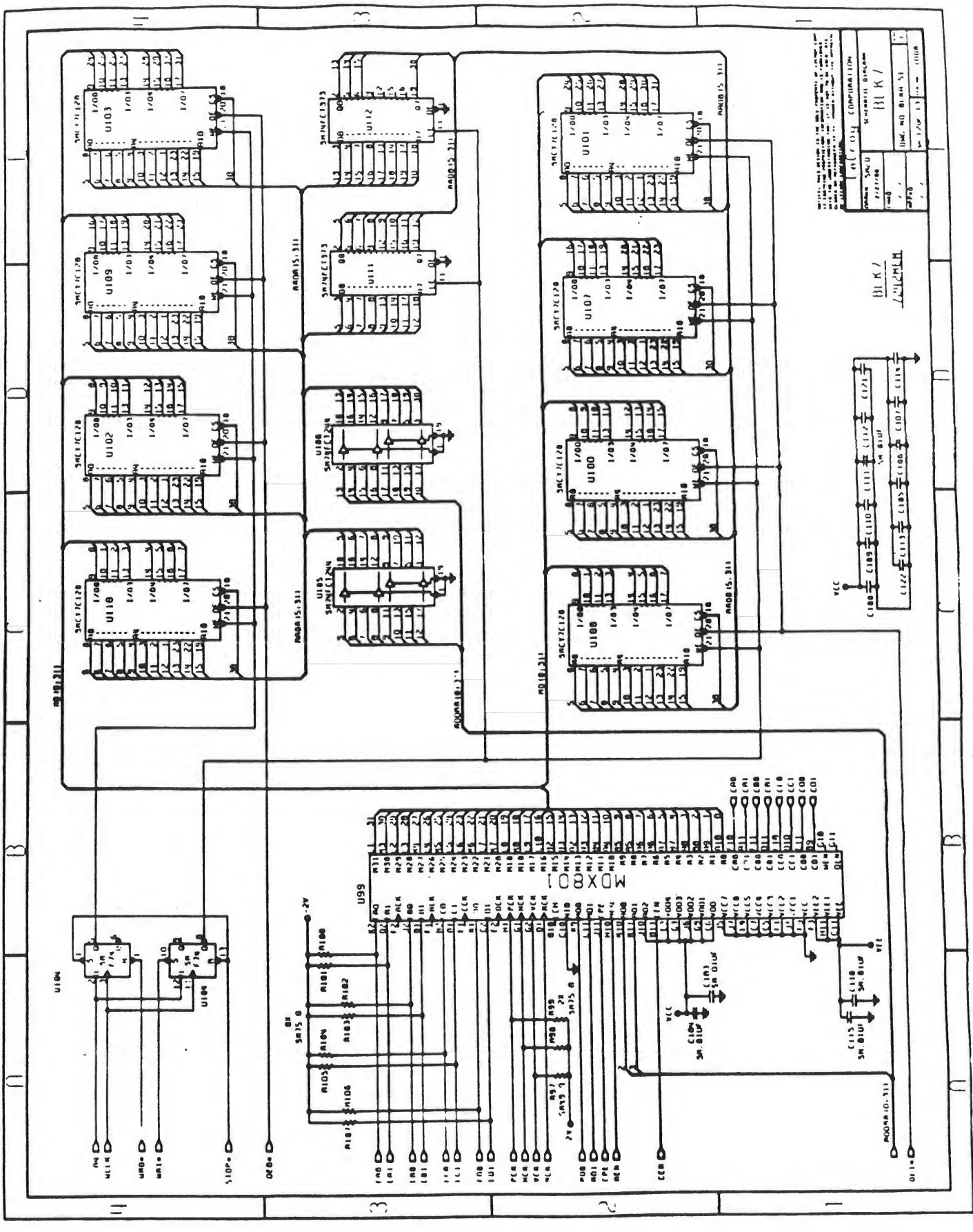

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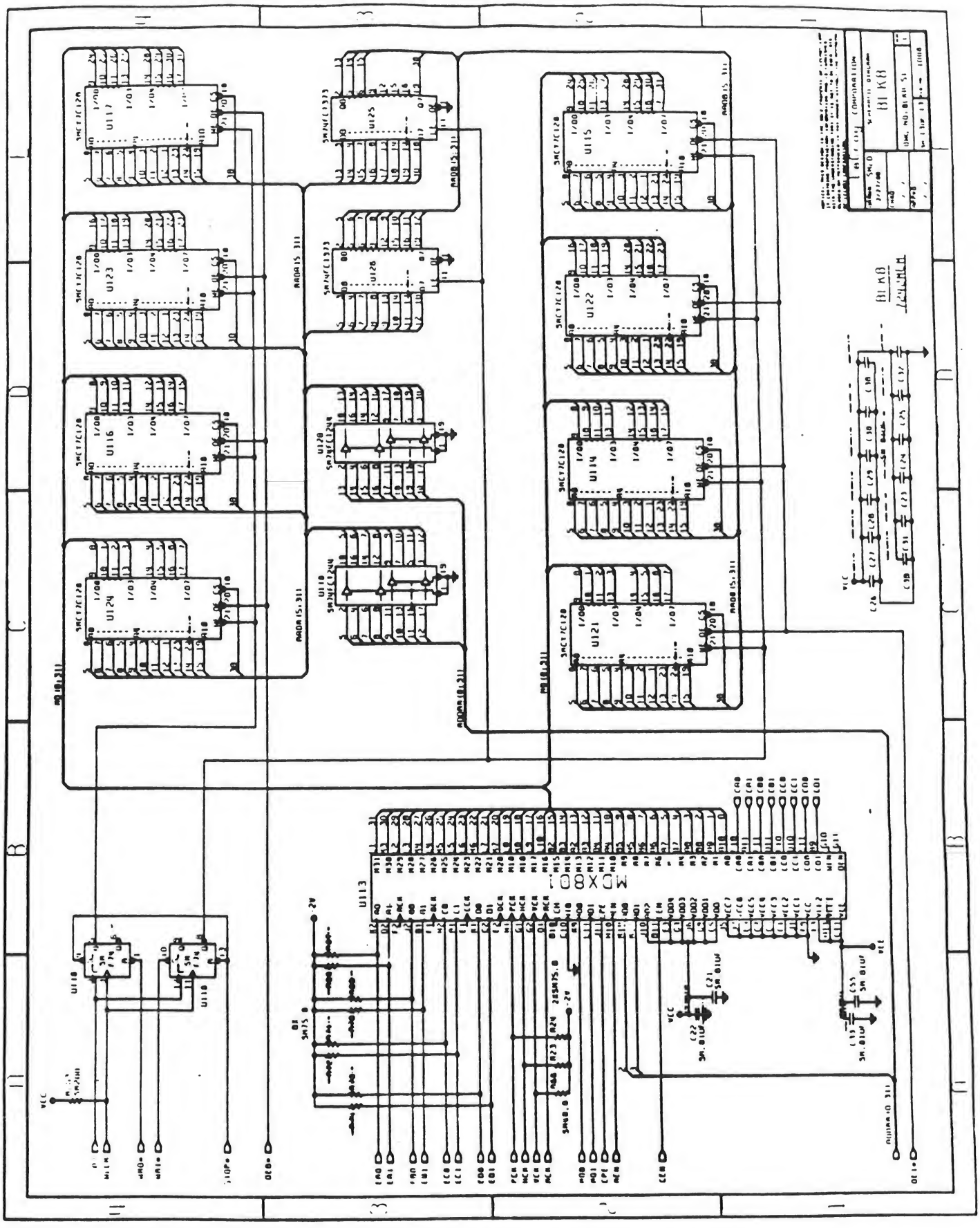

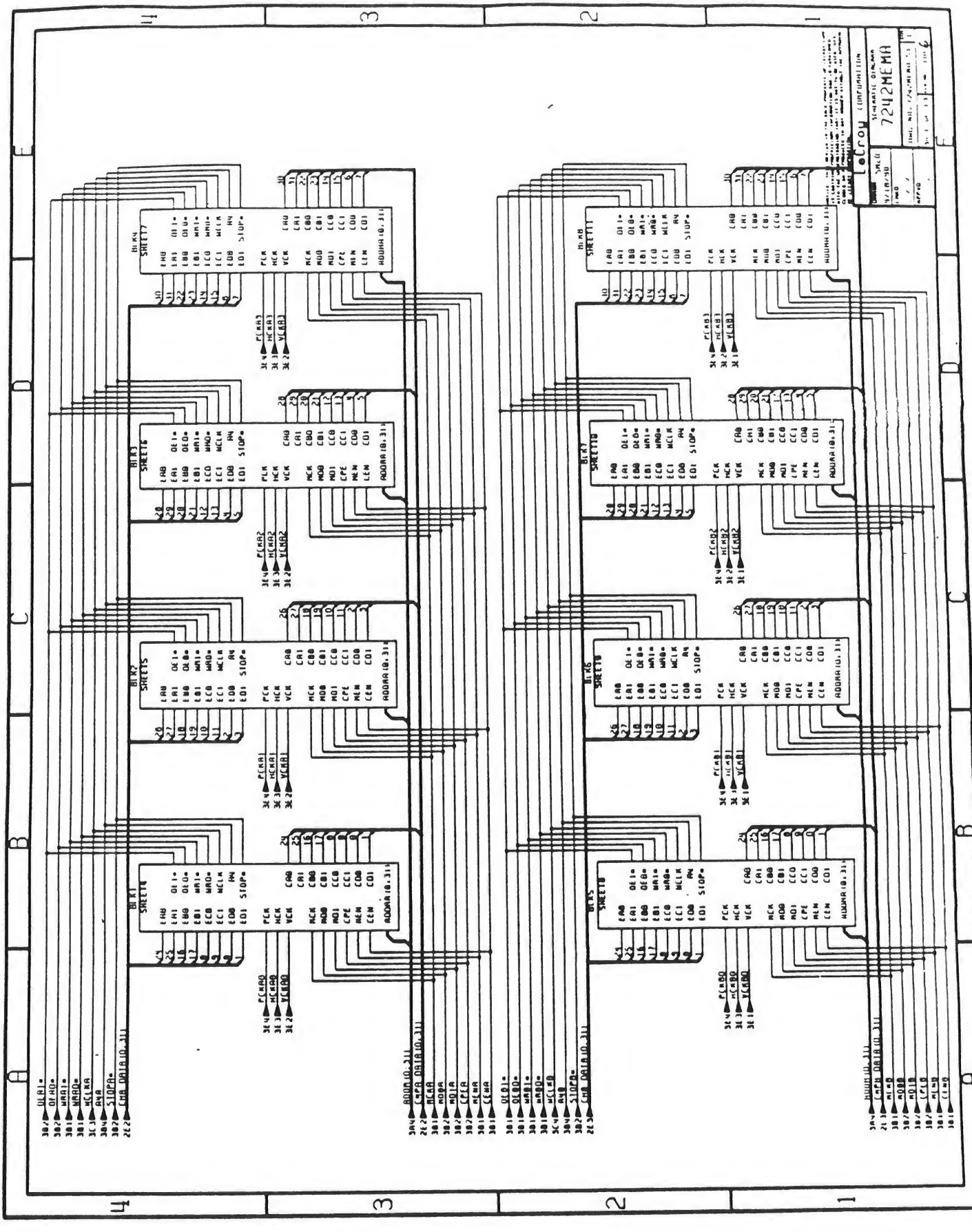

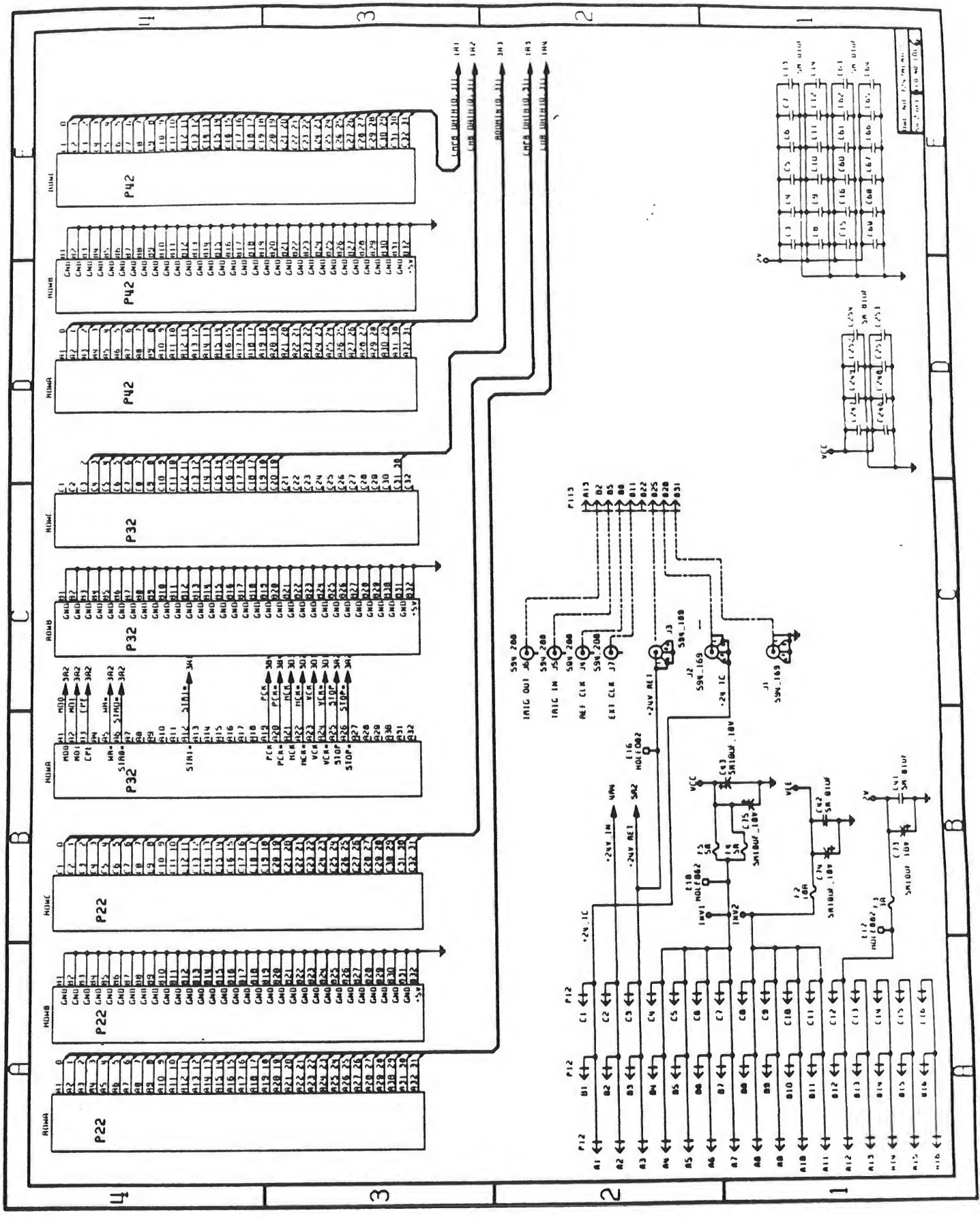

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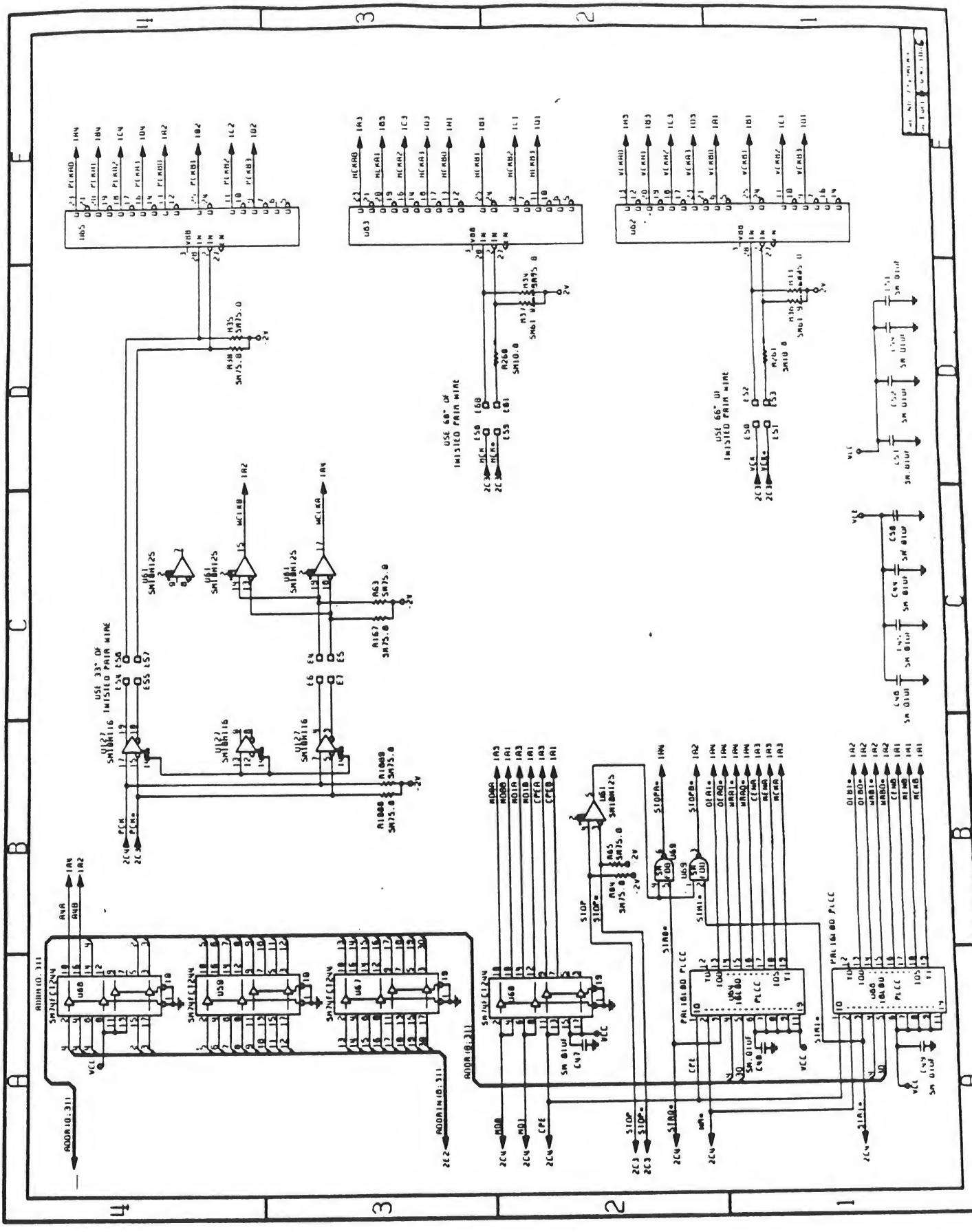

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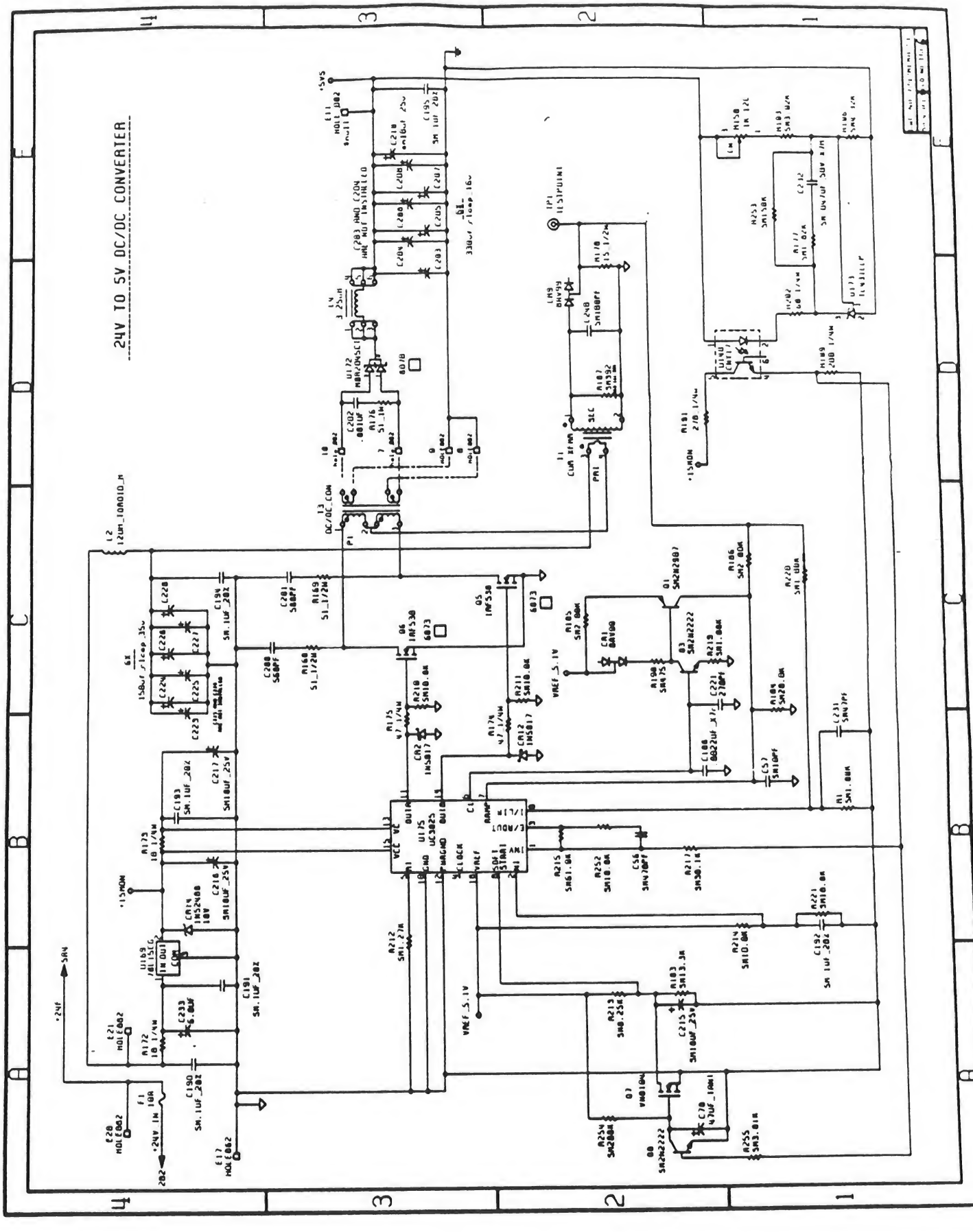
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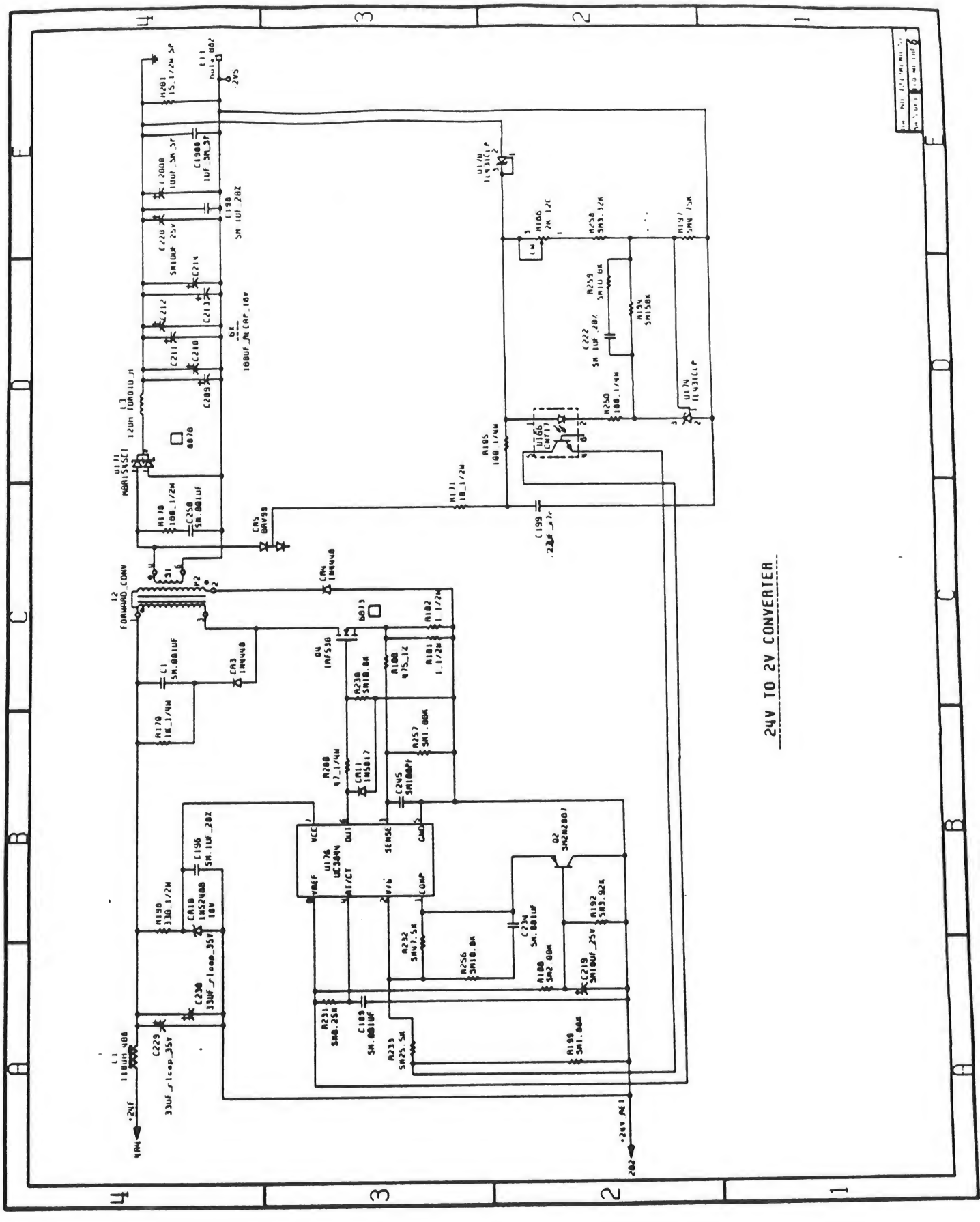
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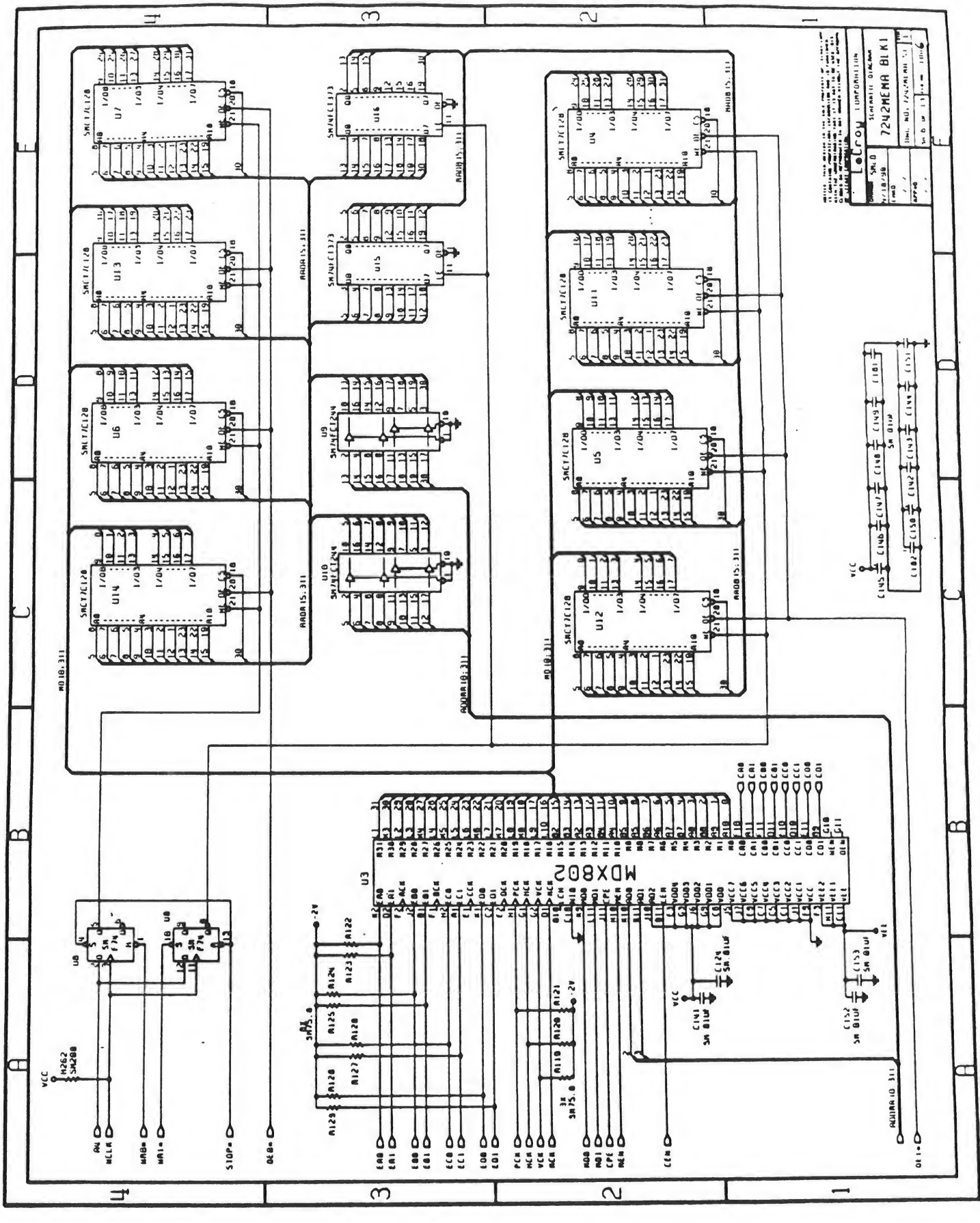

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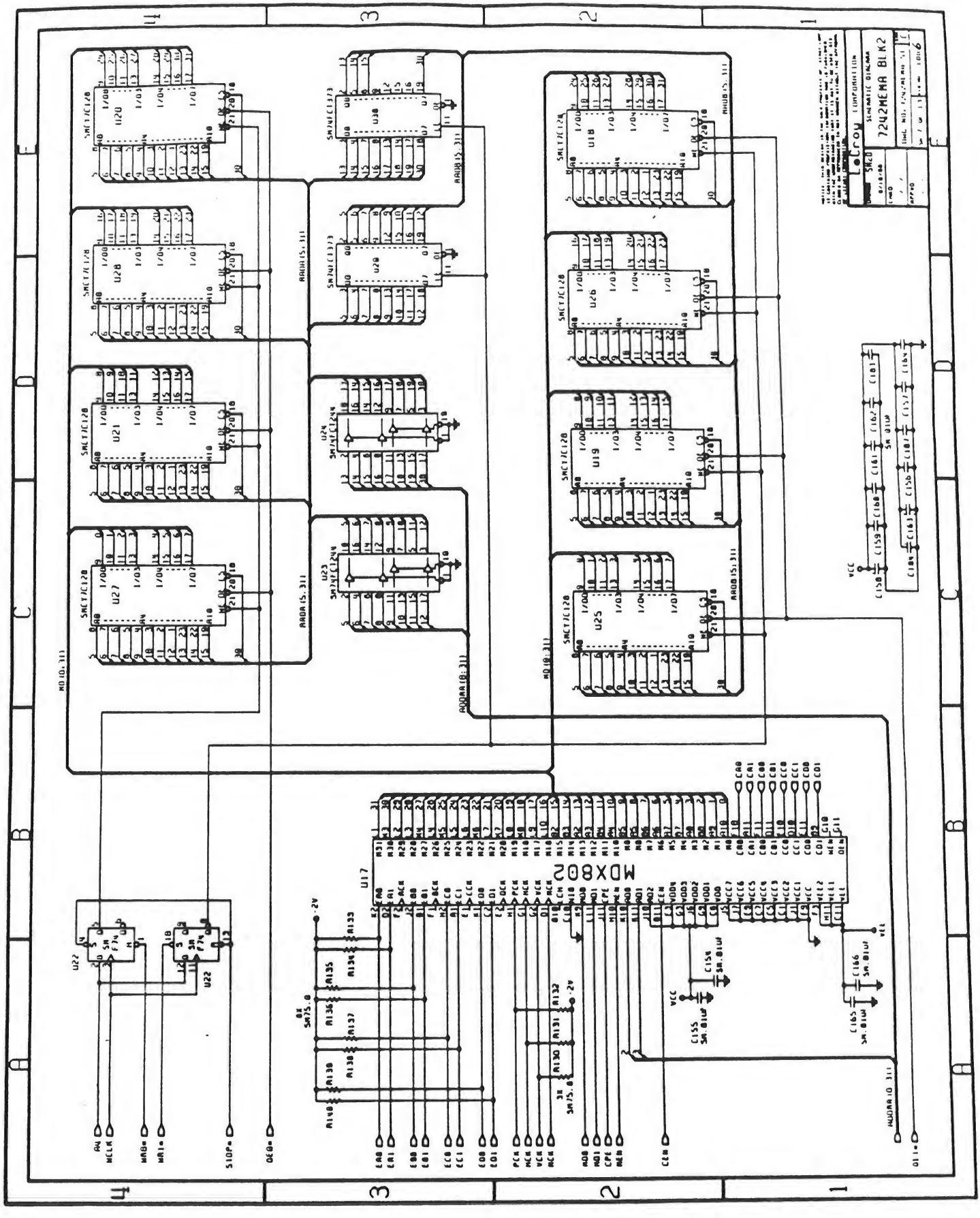

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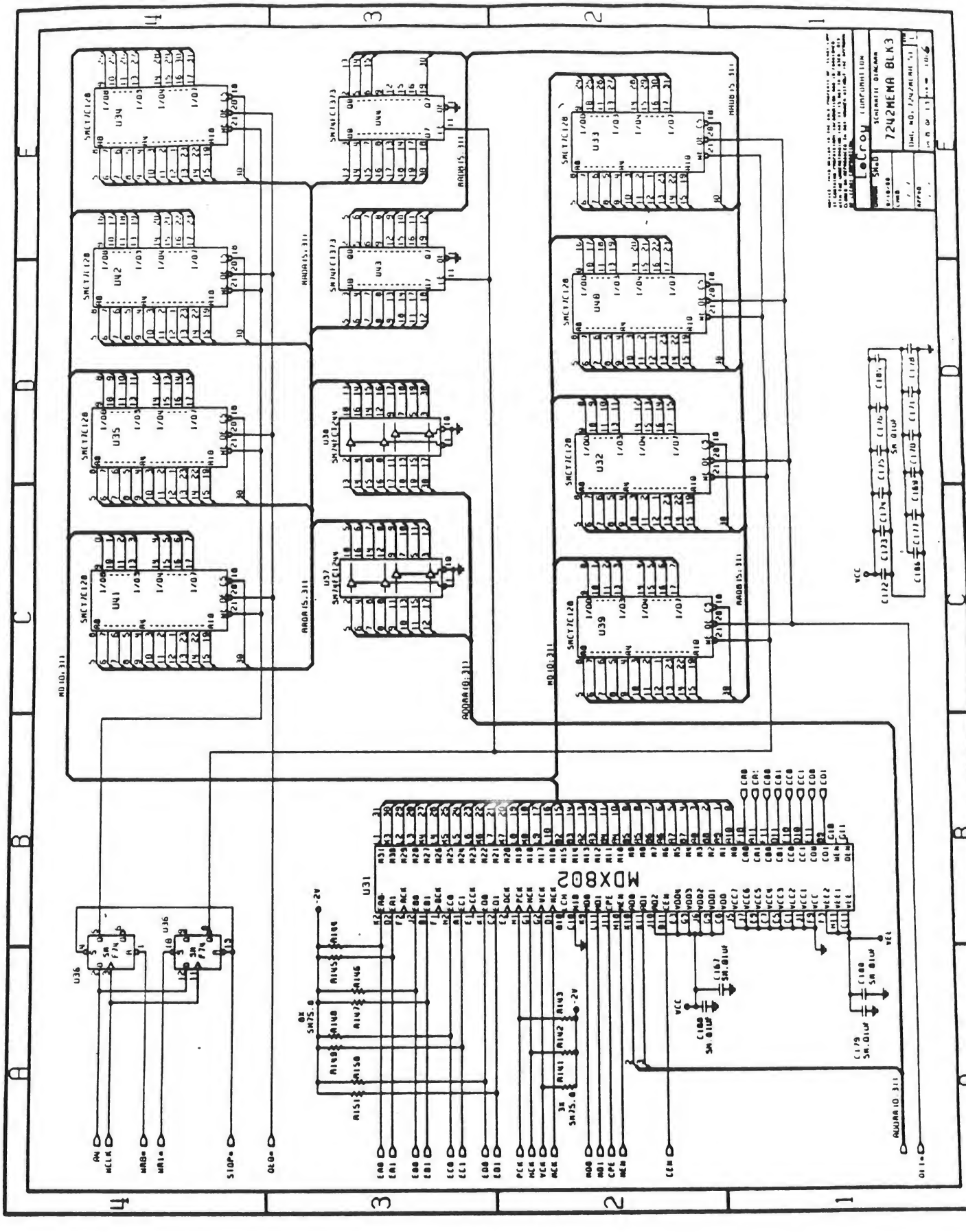

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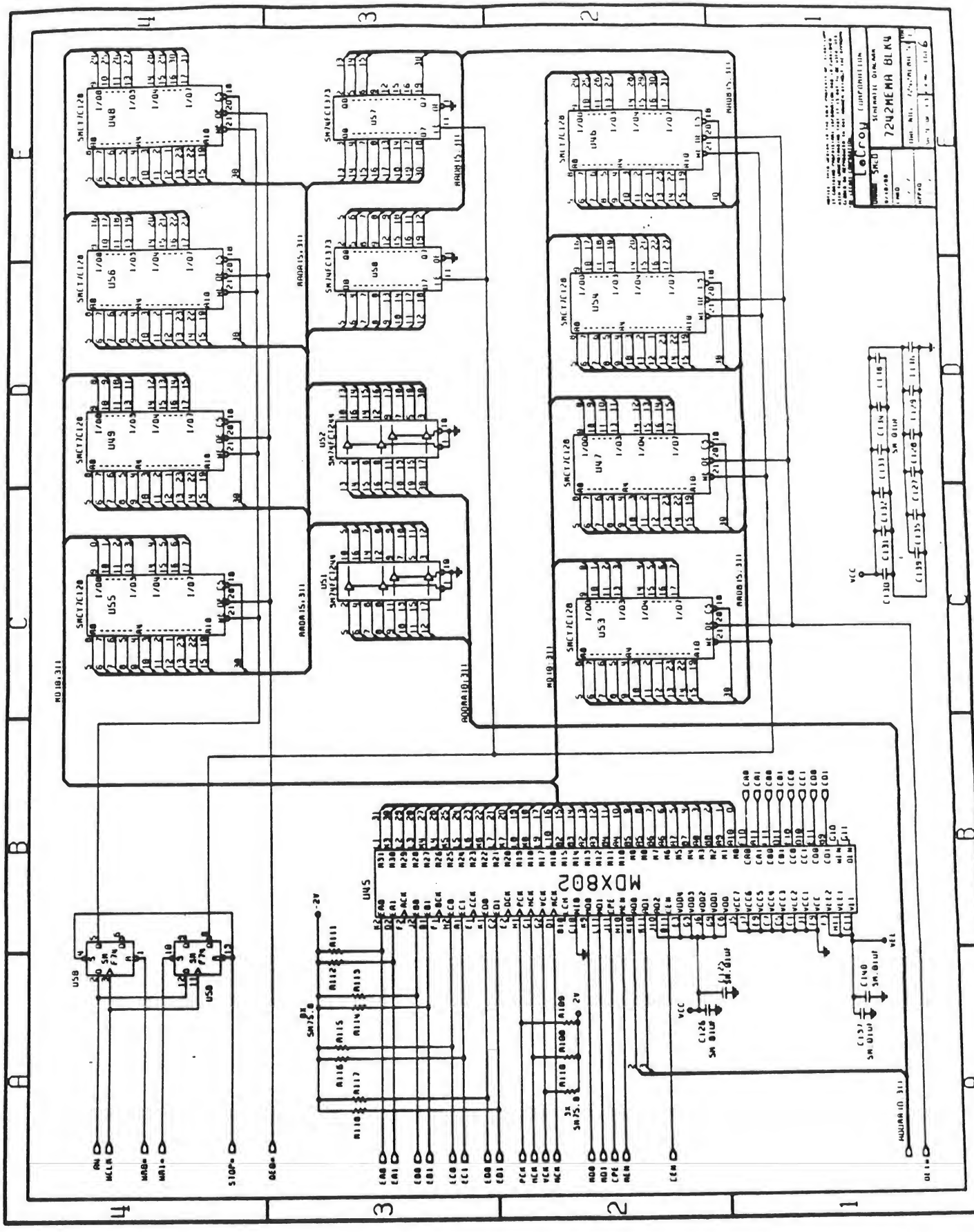

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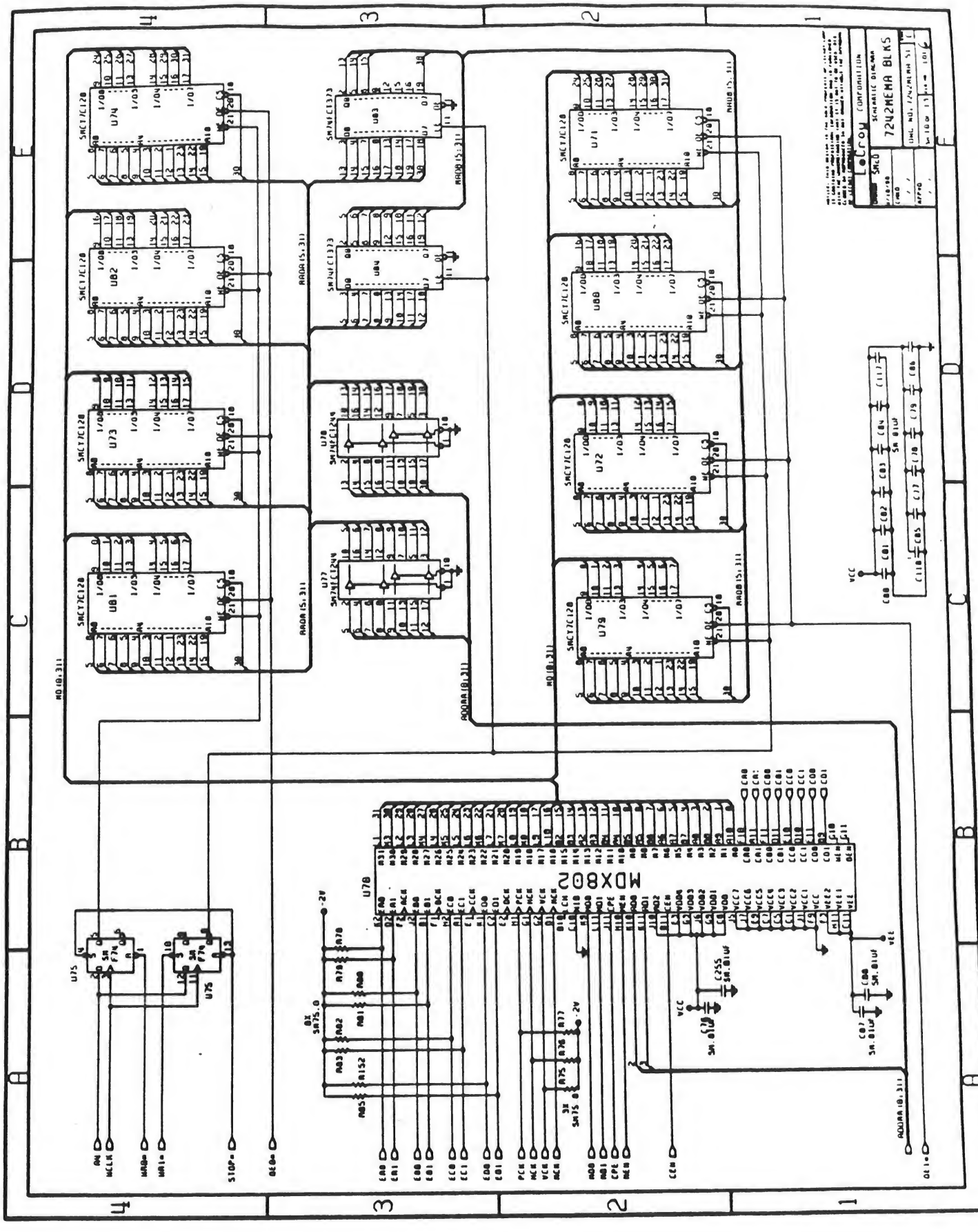

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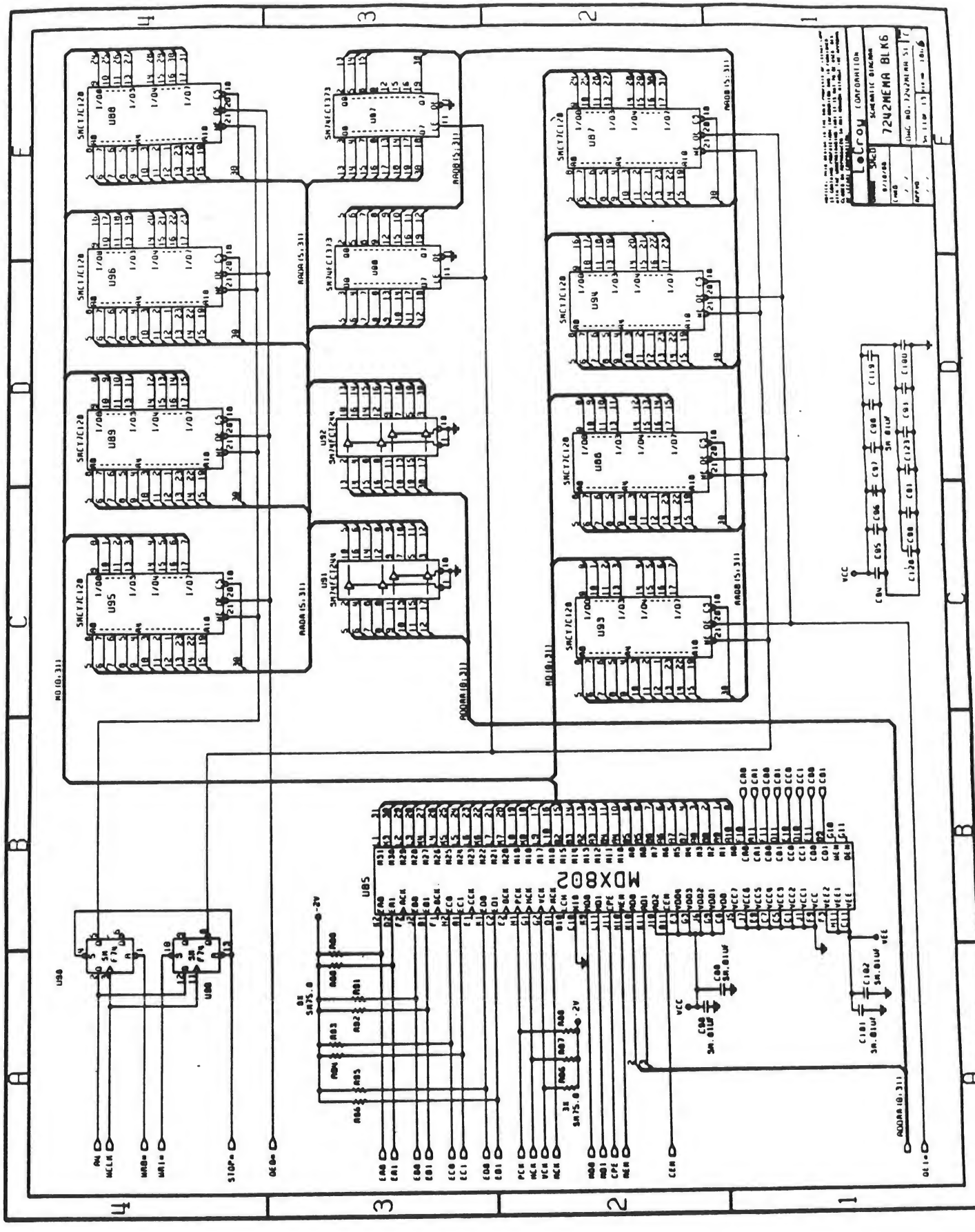
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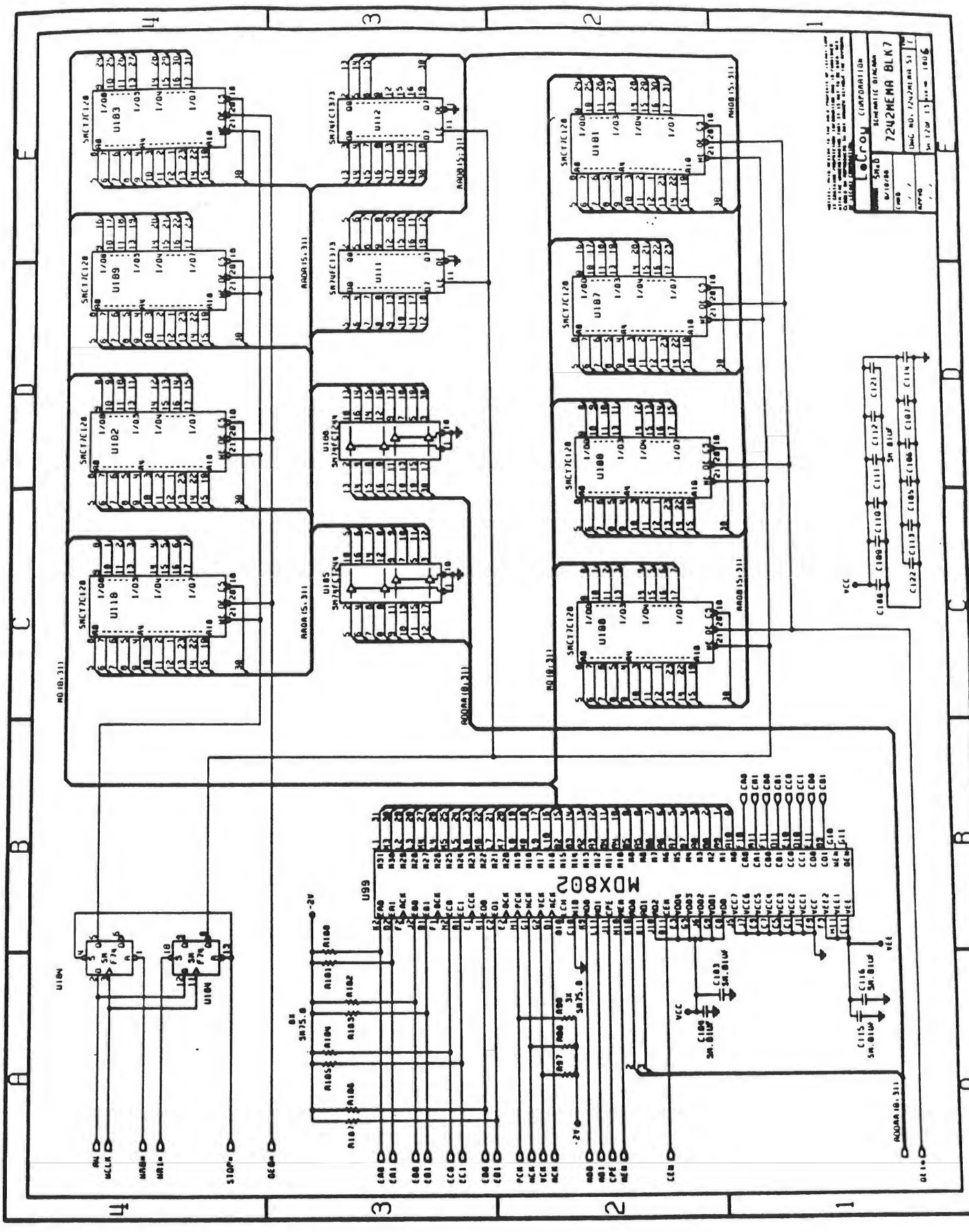
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U184
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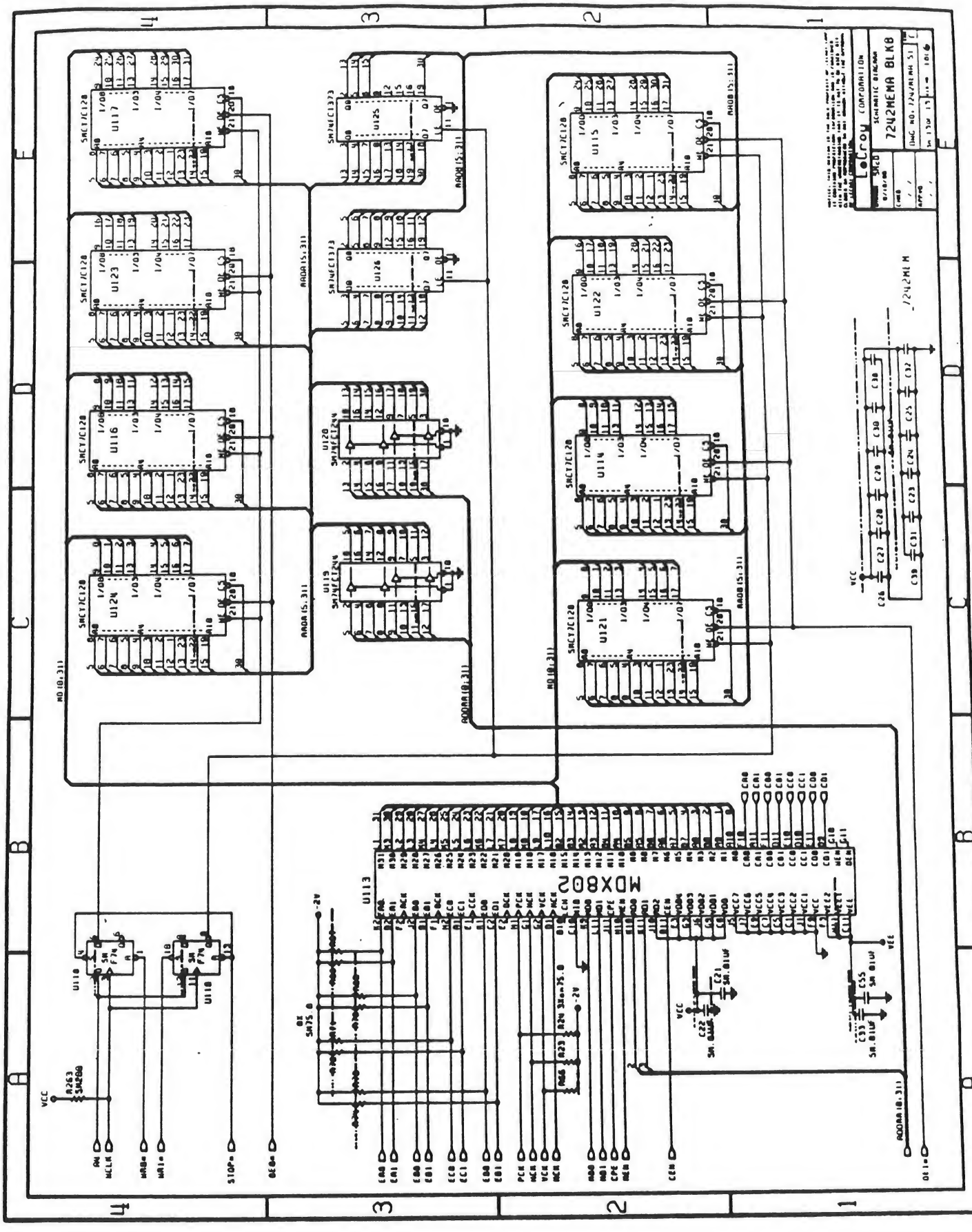

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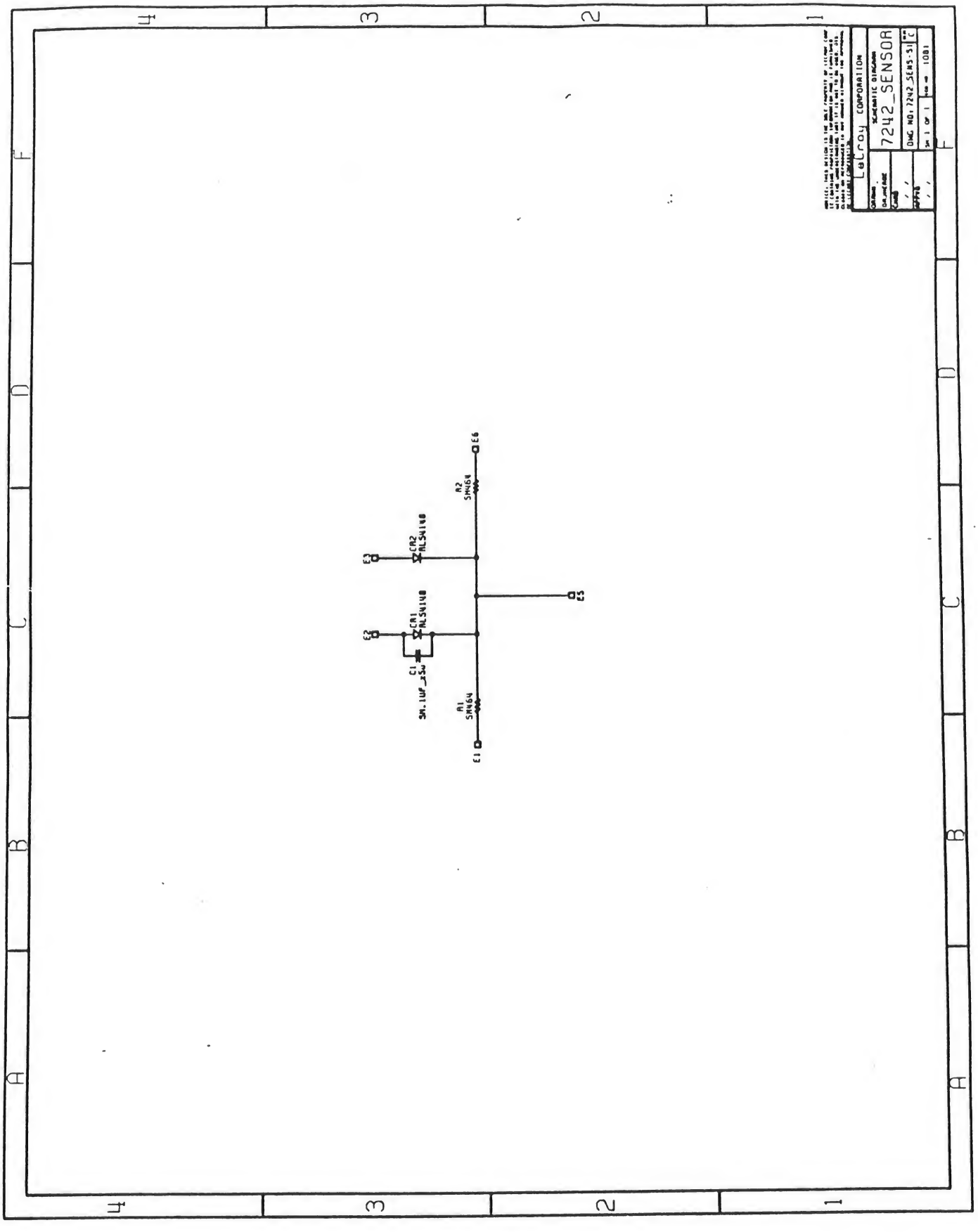
LeCroy CORPORATION
SCHEMATIC DIAGRAM
7242_SENSOR
DWG NO: 7242_SENS-S1
SH 1 OF 1
1001
E1
E2
E3
E5
E6
R1
SM464
R2
SM464
CR1
RLS4148
CR2
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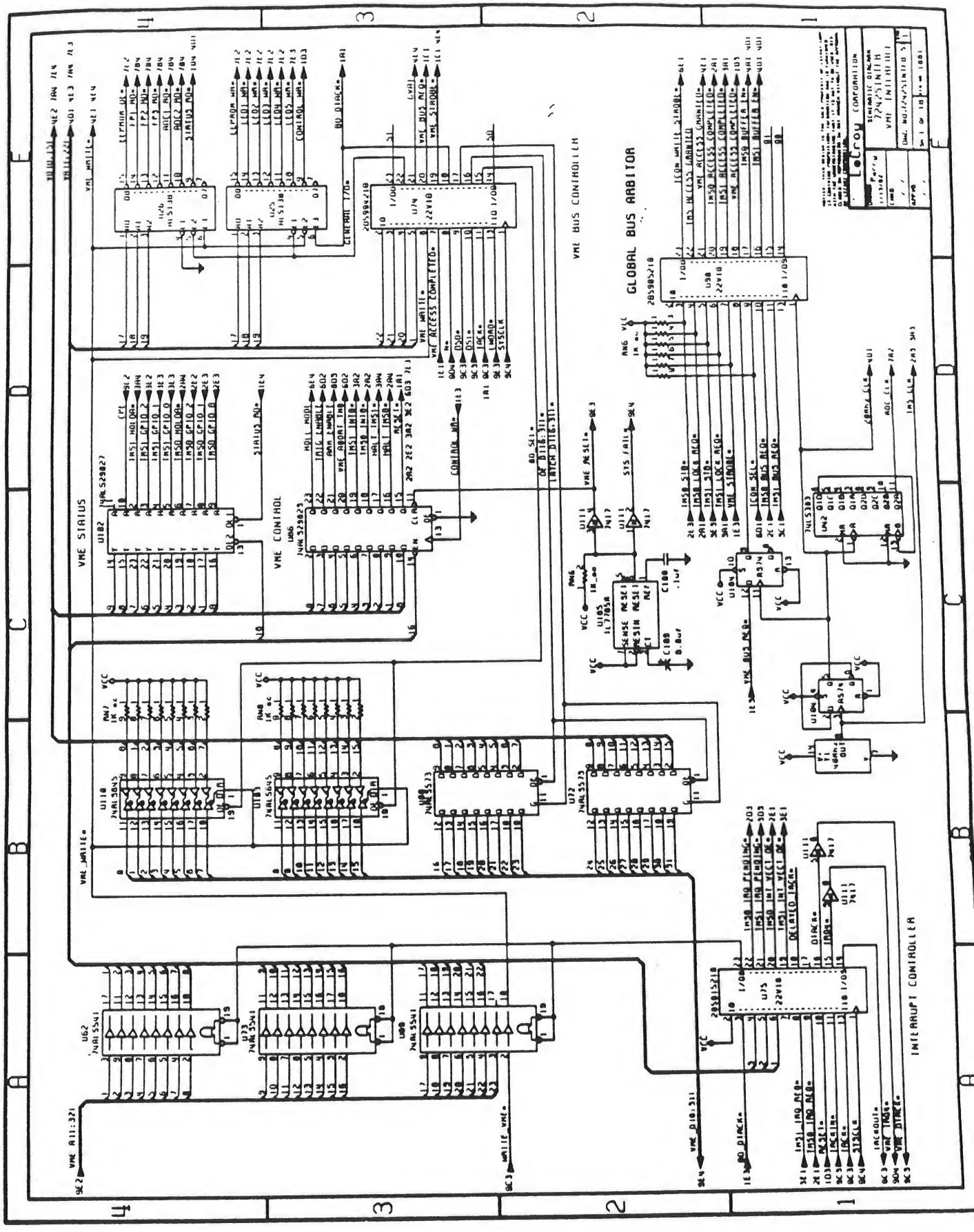
C1
SM.1UF_xSW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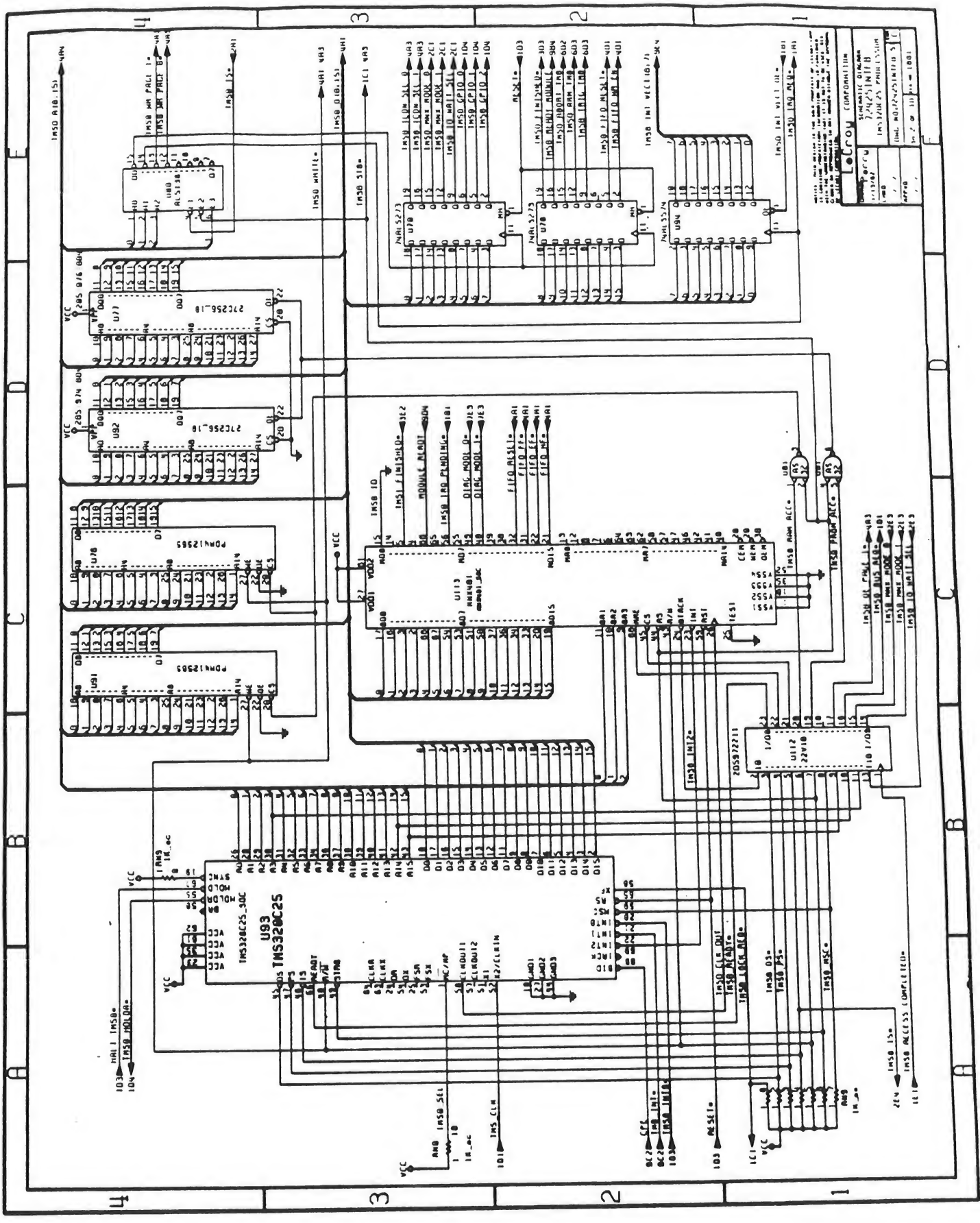
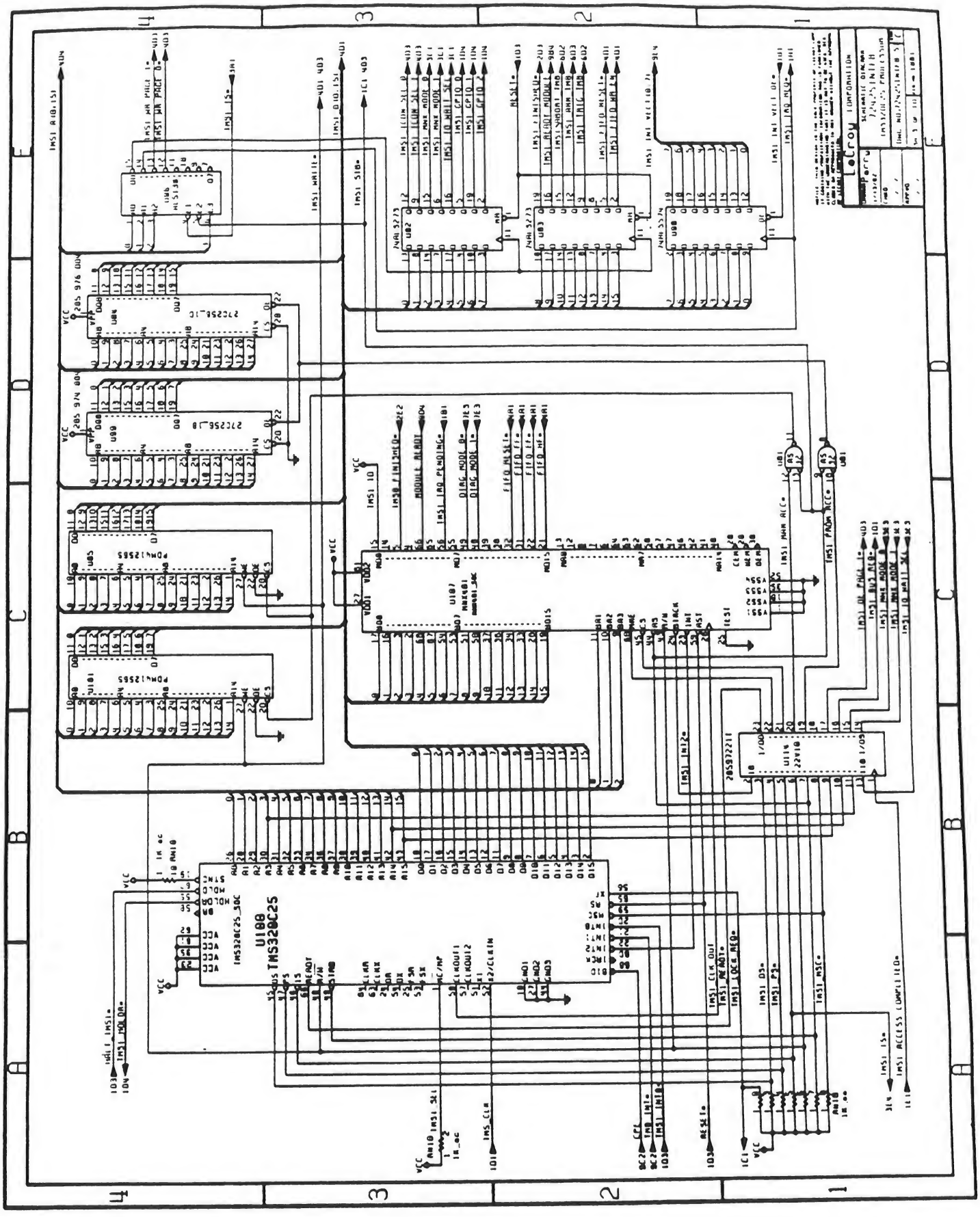
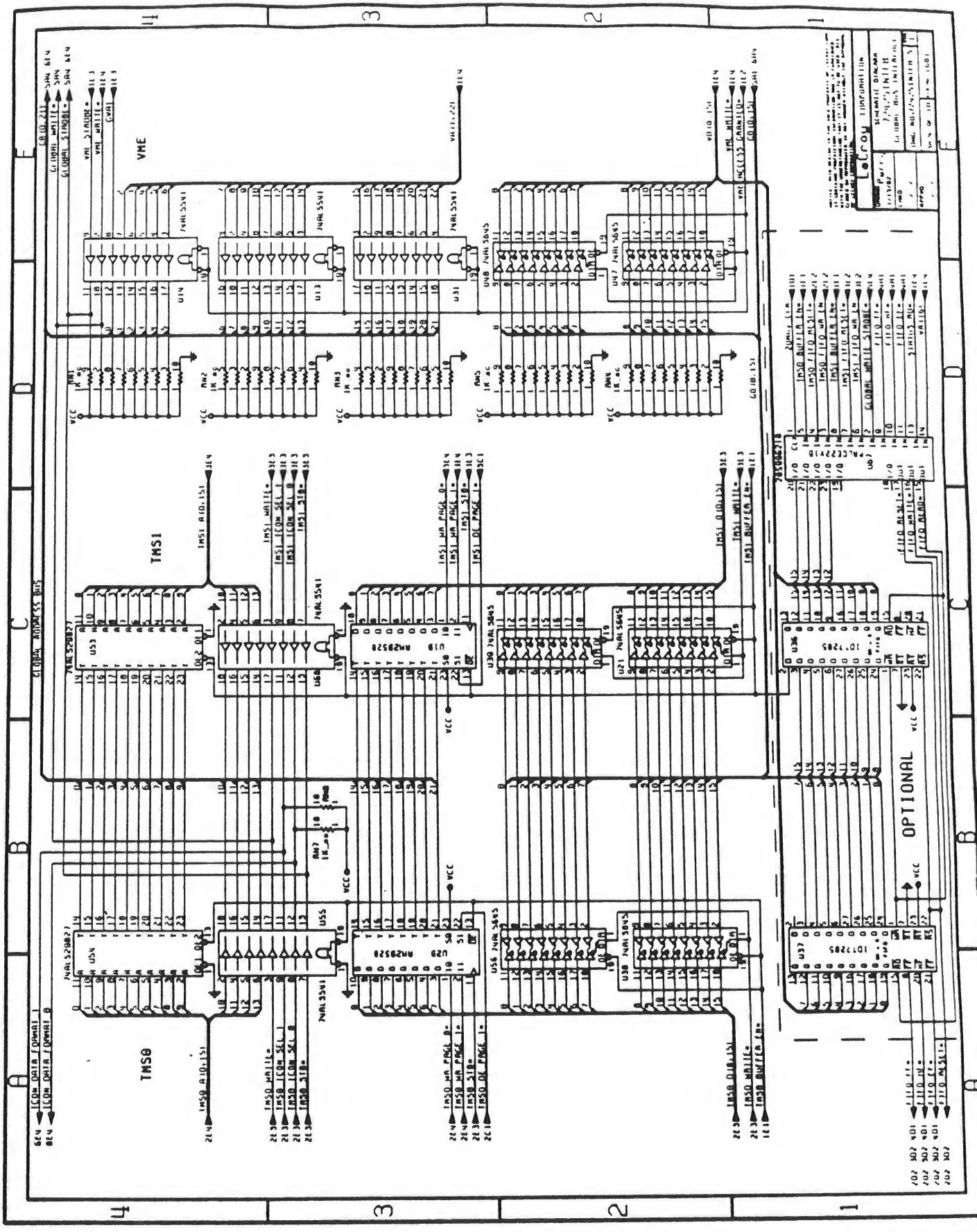
VME CONTROL
VME BUS CONTROLLER
GLOBAL BUS ARBITOR
INTERRUPT CONTROLLER



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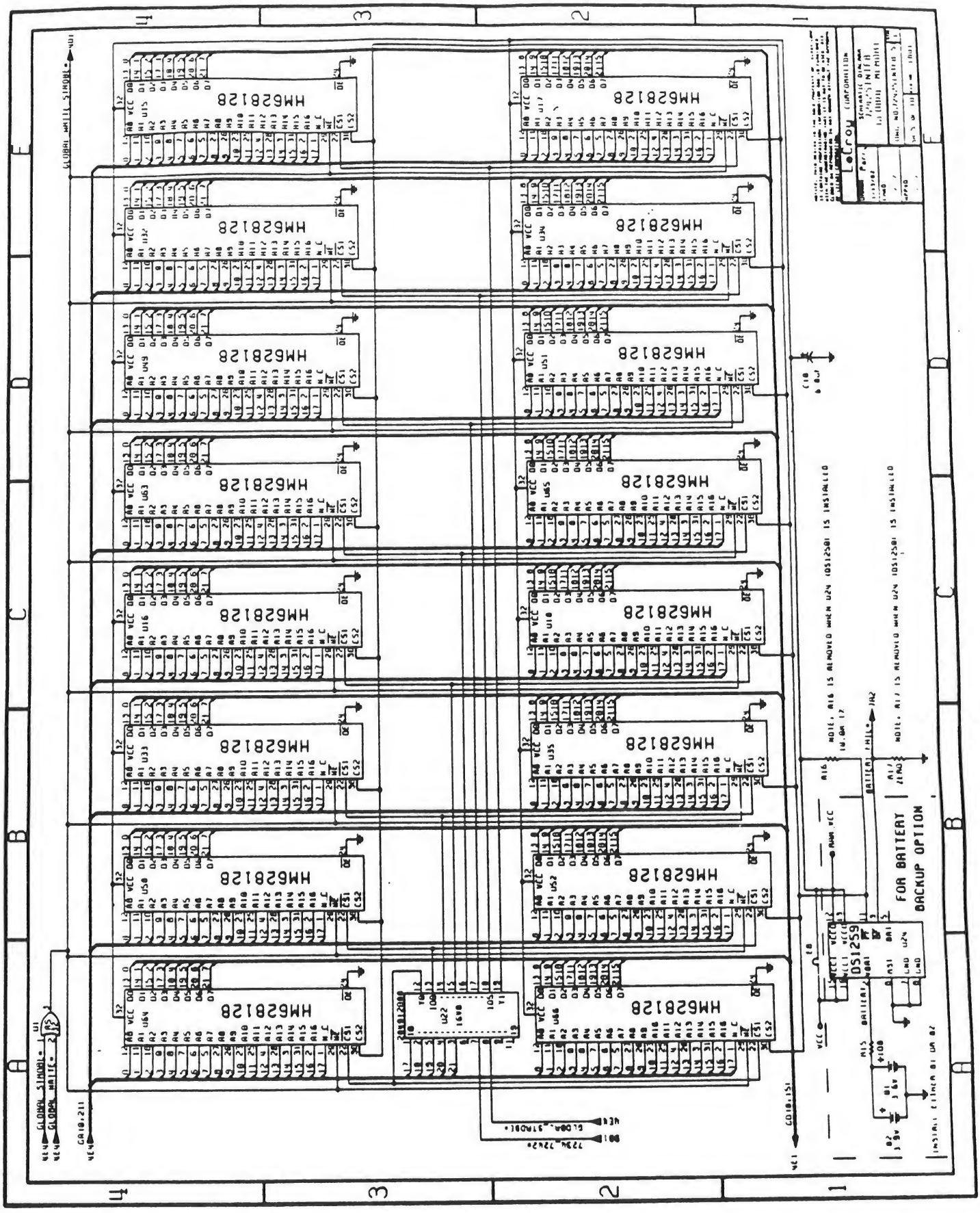
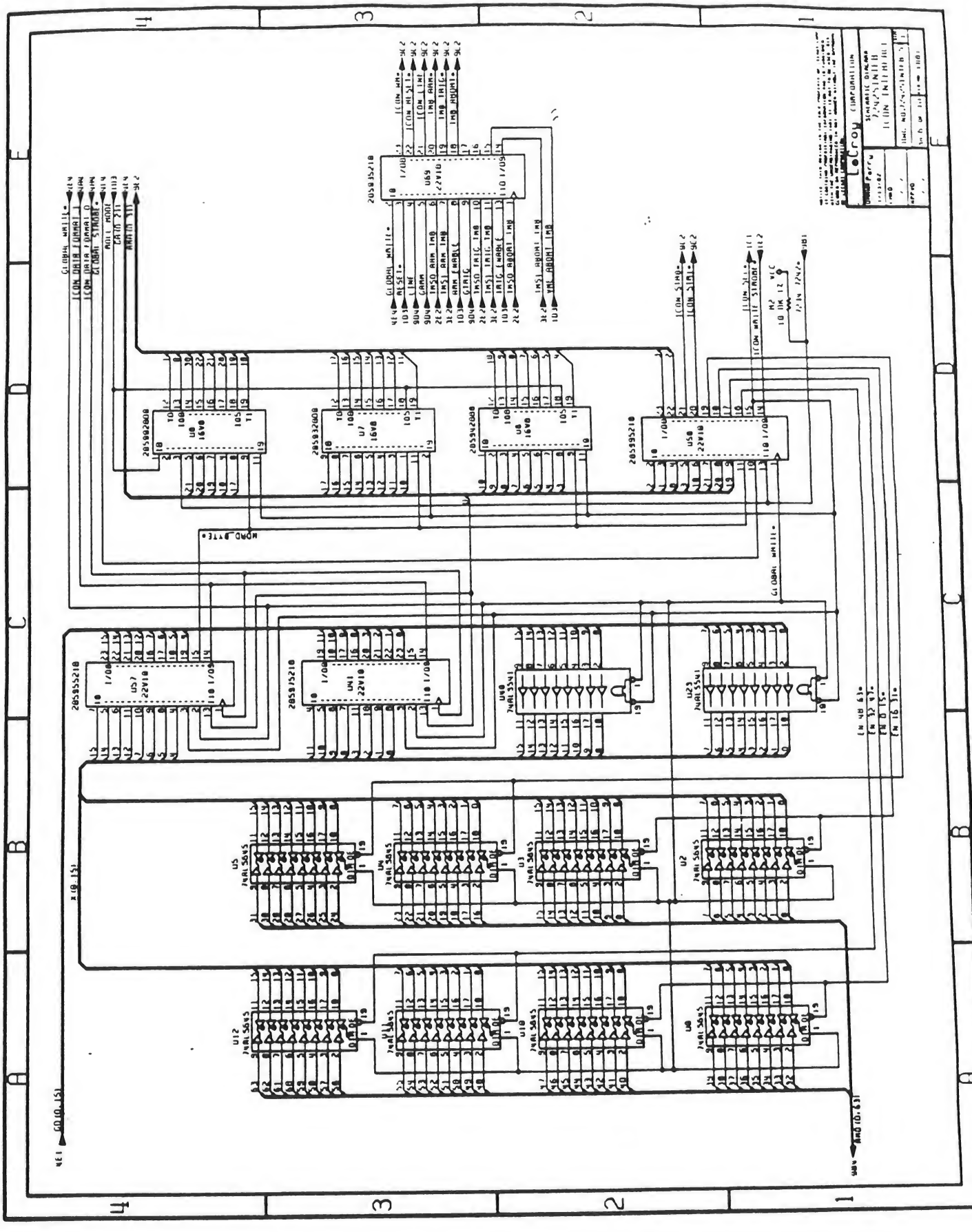
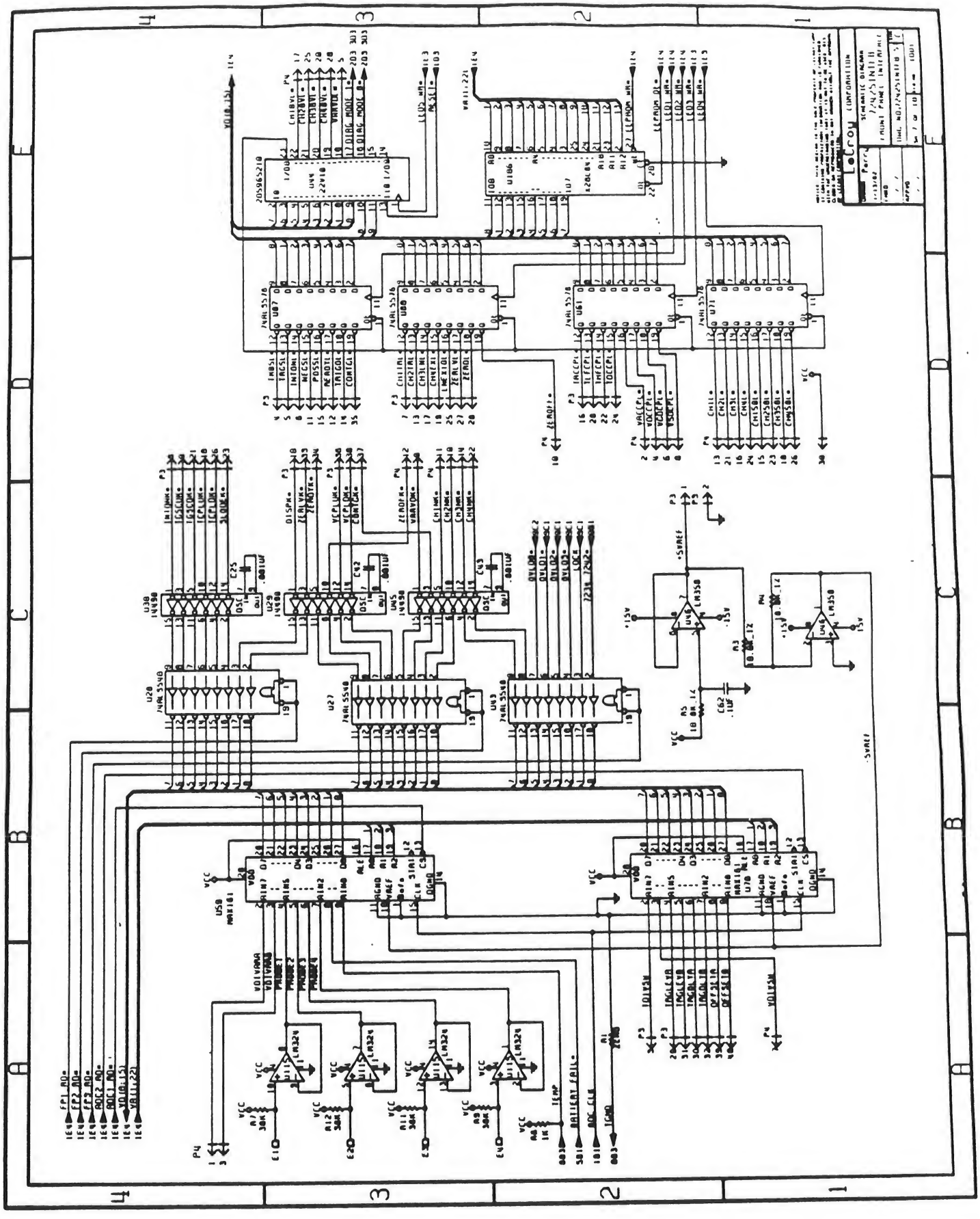
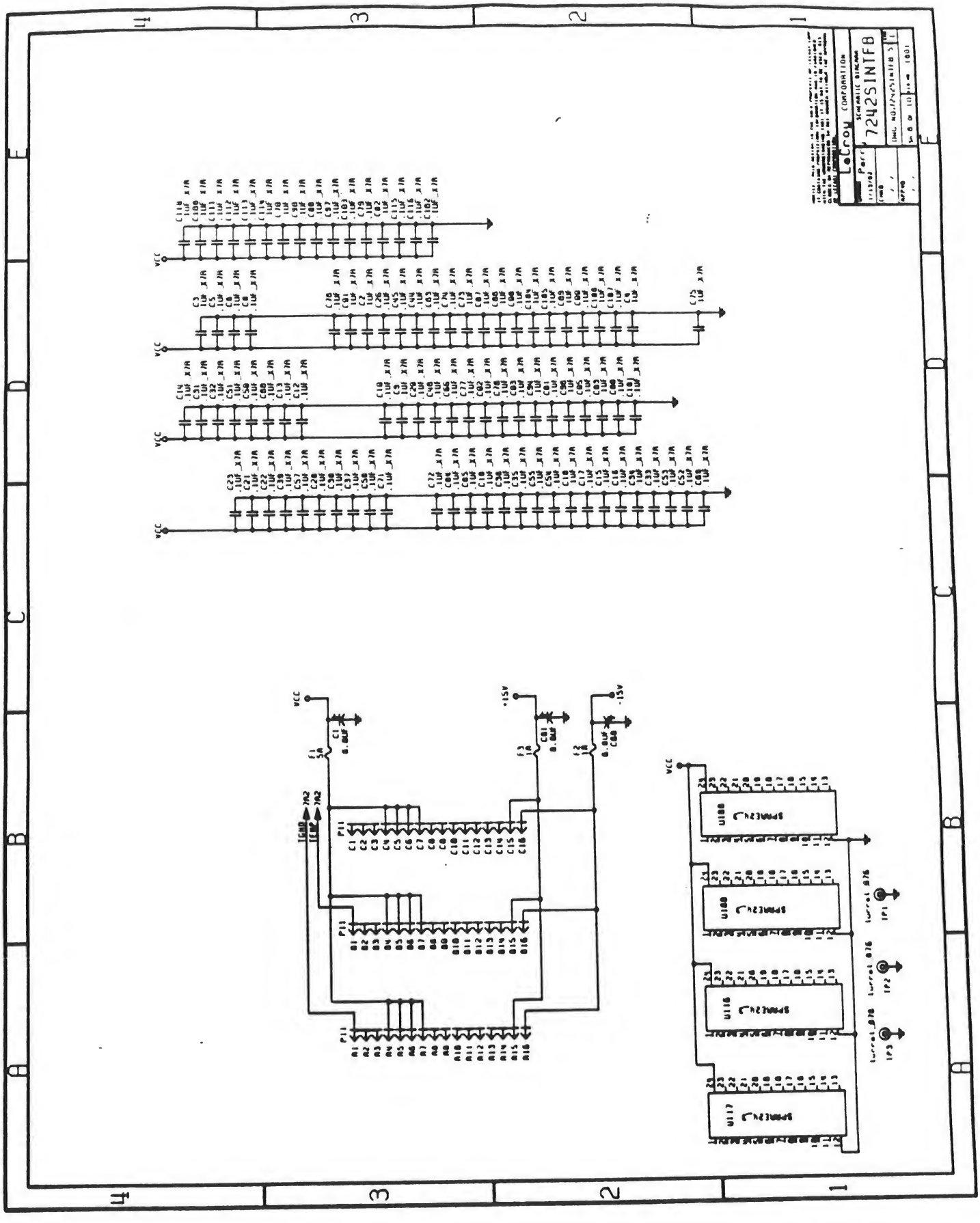
TMS1
TMS0
OPTIONAL

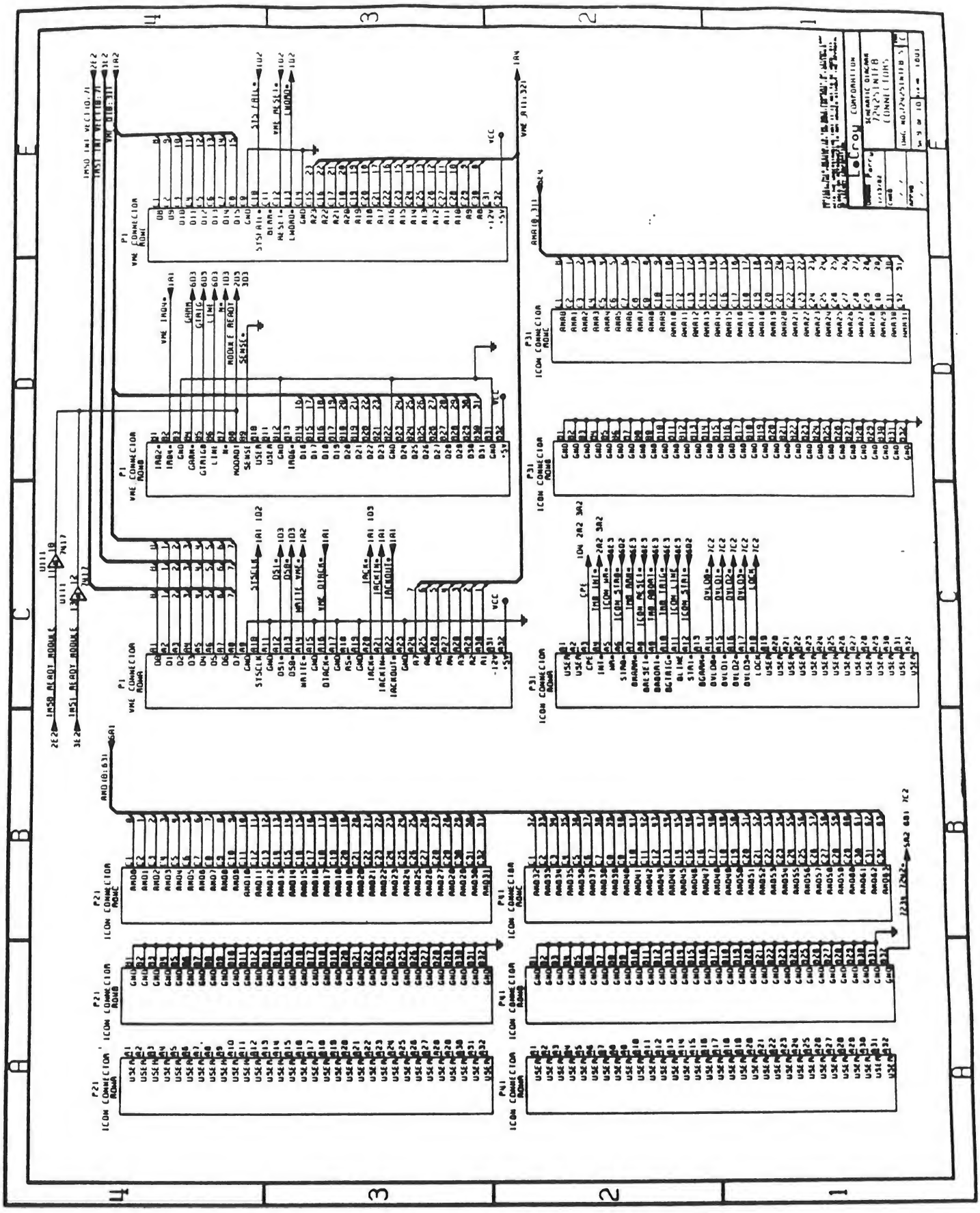


7242SINTFB **Sheet 5.**









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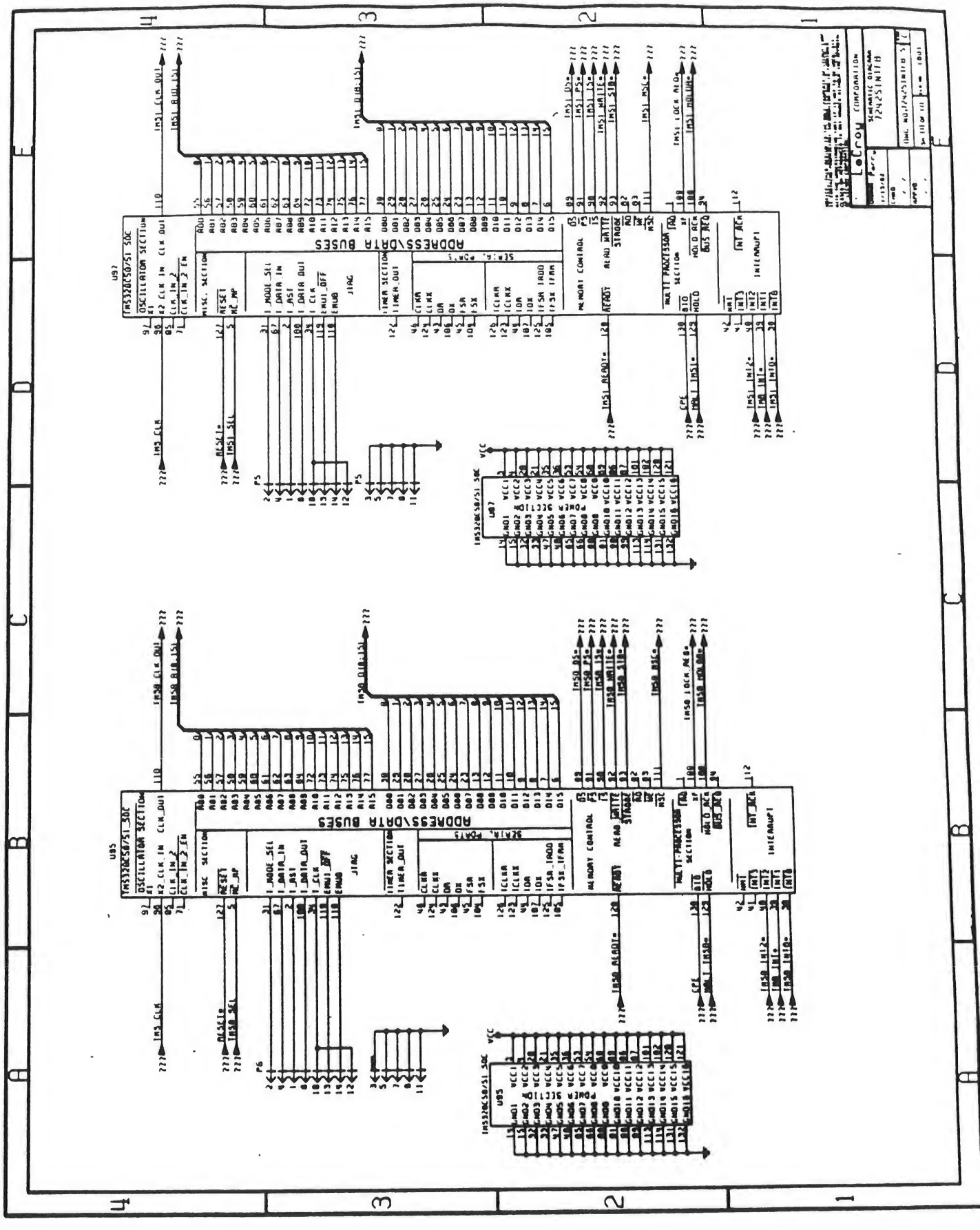
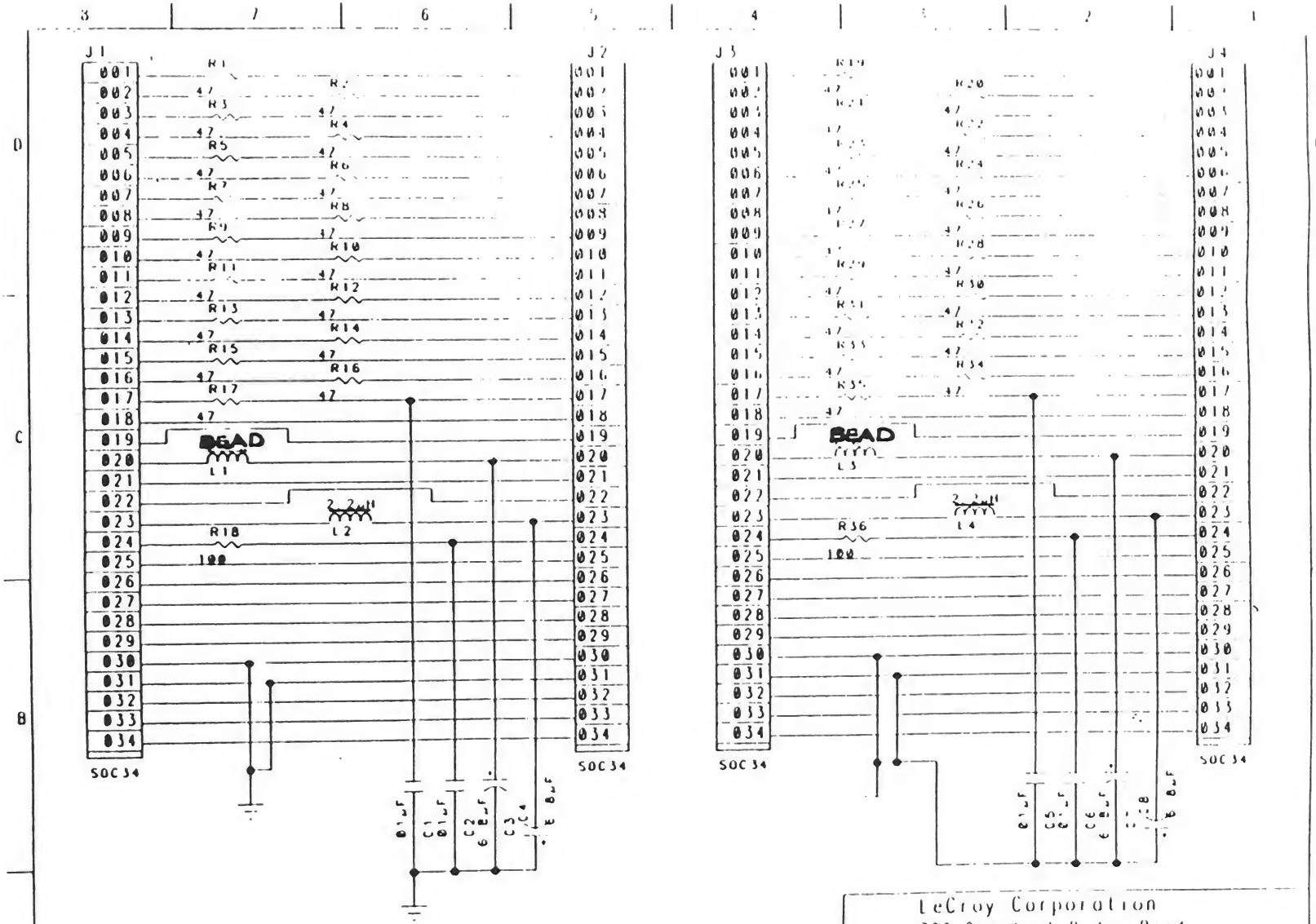




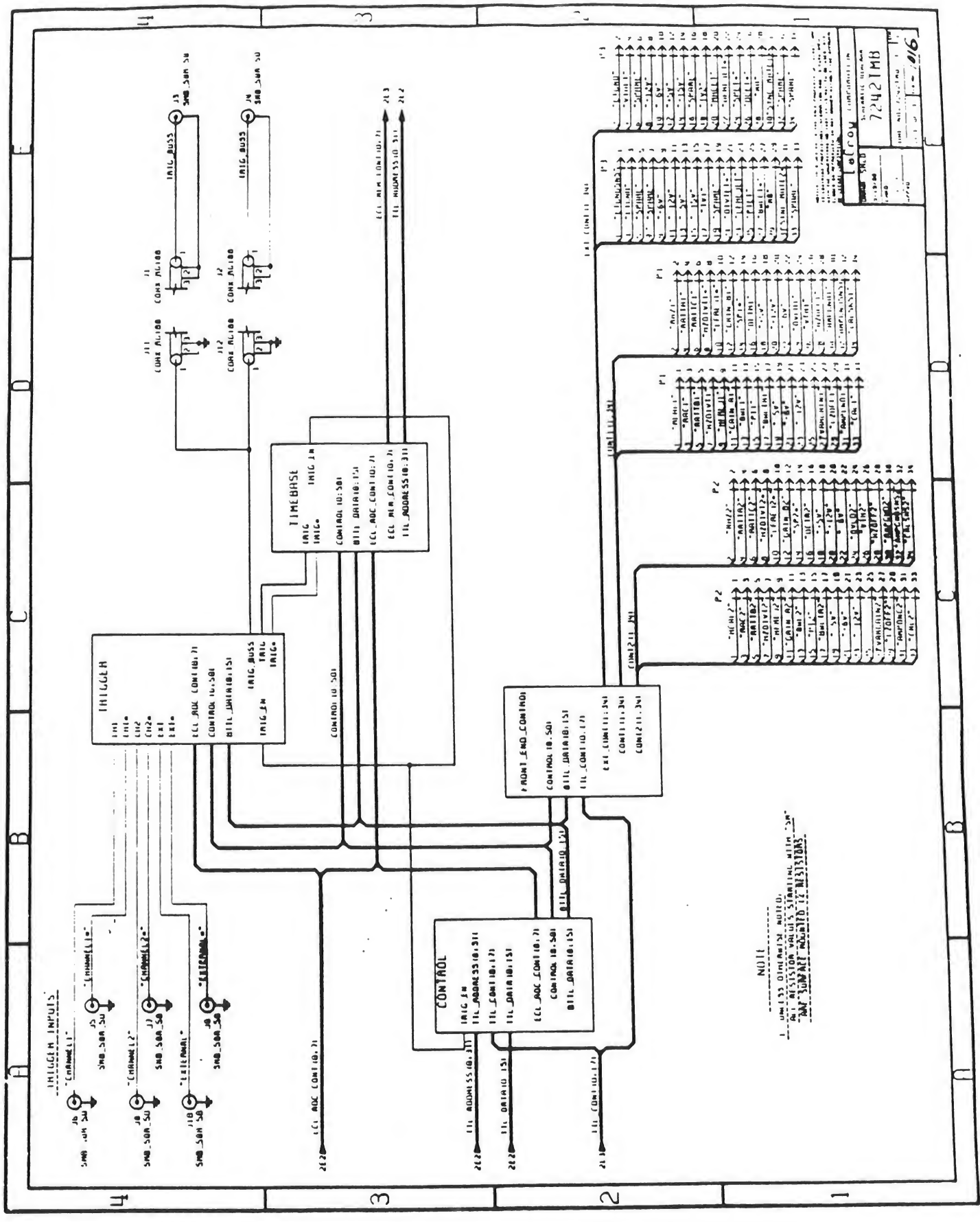
All resistors 1/8watt through hole
All capacitors through hole
Ground plane on component side, signals on solder side.
Connectors are LeCroy number 454320034

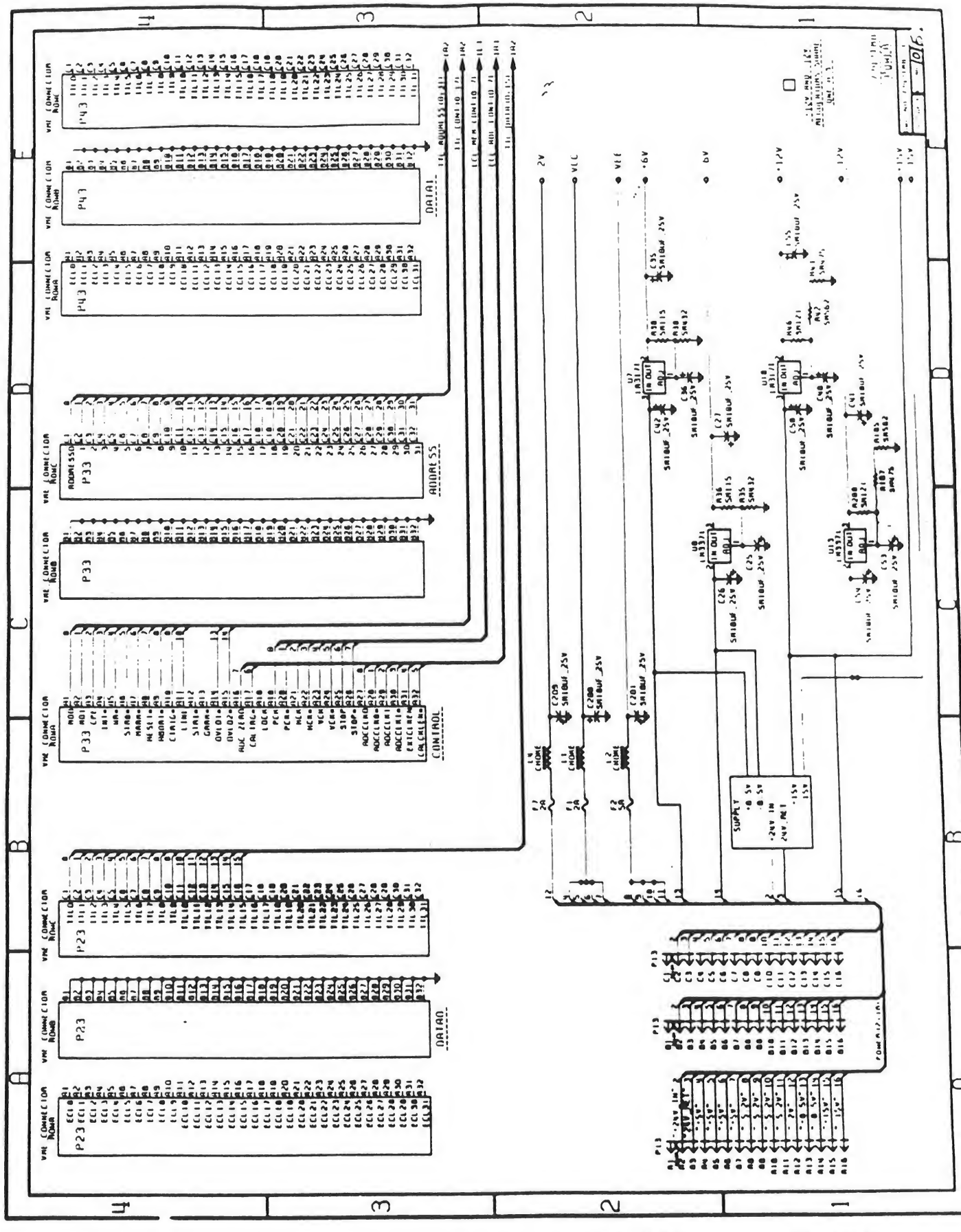
LeCroy Corporation
700 Chestnut Ridge Road
Chestnut Ridge, NY 10977-6499

TITLE
7242TAMP, cable replacement

SIZE	CODE	NUMBER	REV
A		1004	A

PRINT March 19, 1991 | SHEET 1 of 1


TRIGGER
TIMEBASE
CONTROL
FRONT_END_CONTROL
TRIGGER INPUTS
NOTE



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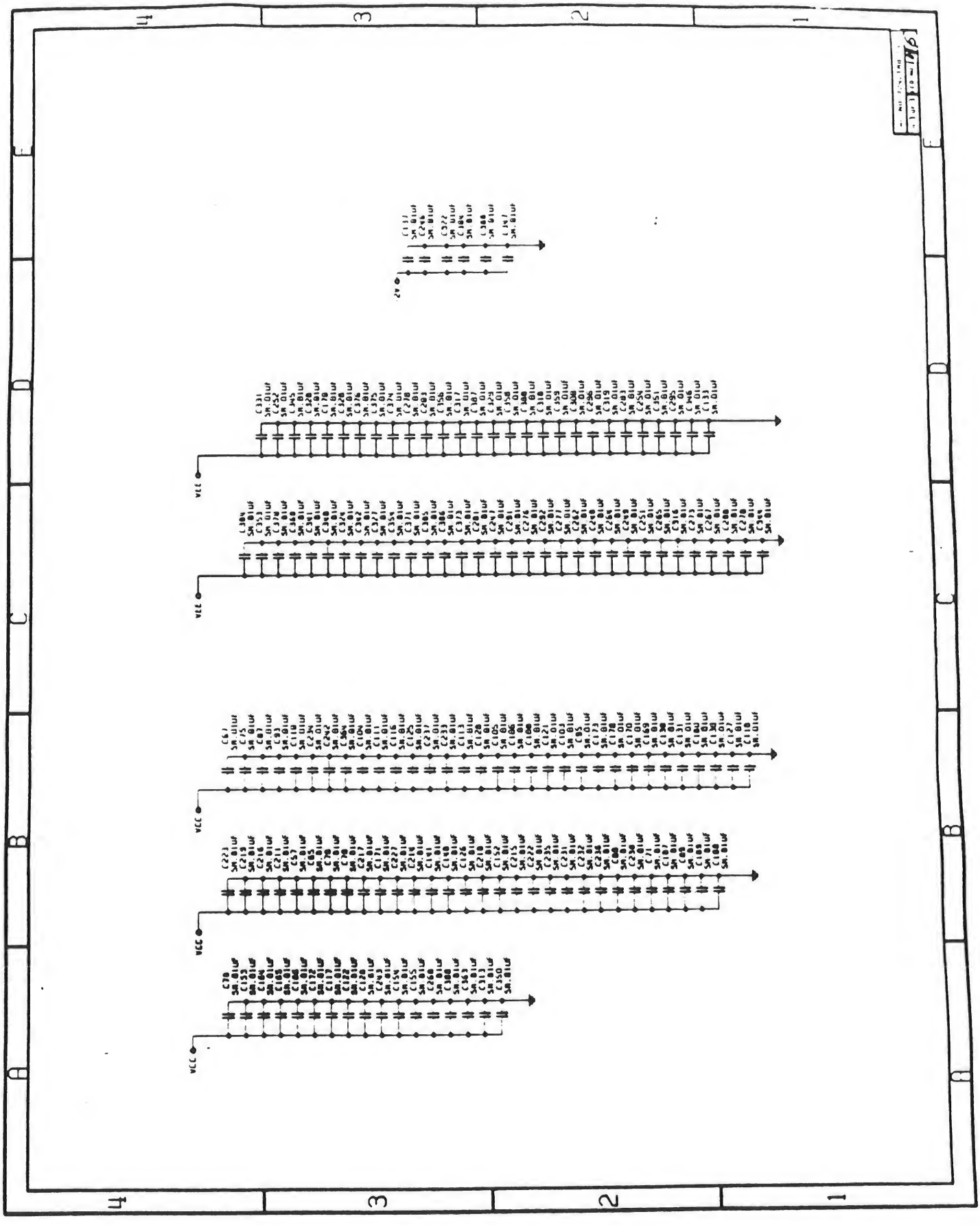

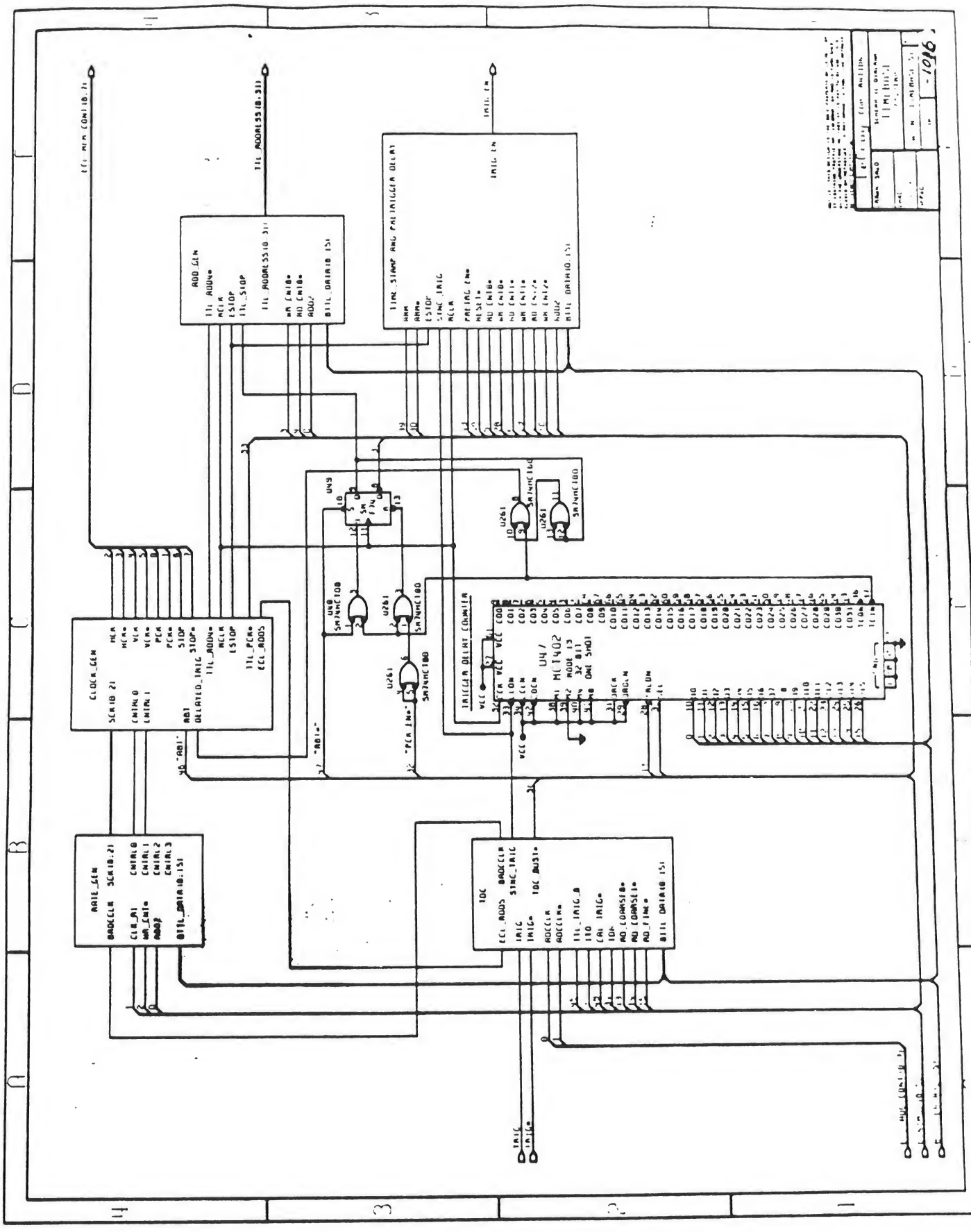

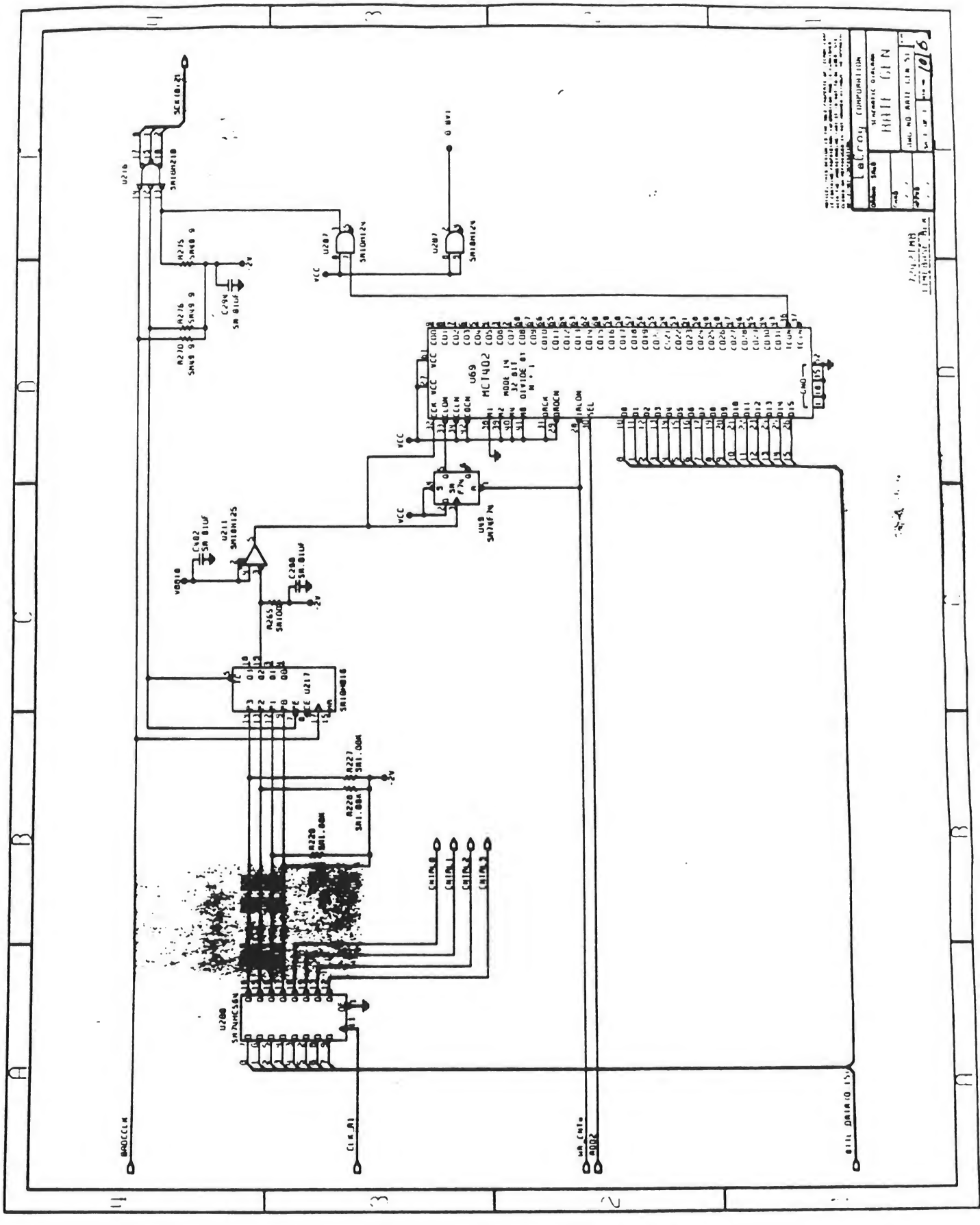

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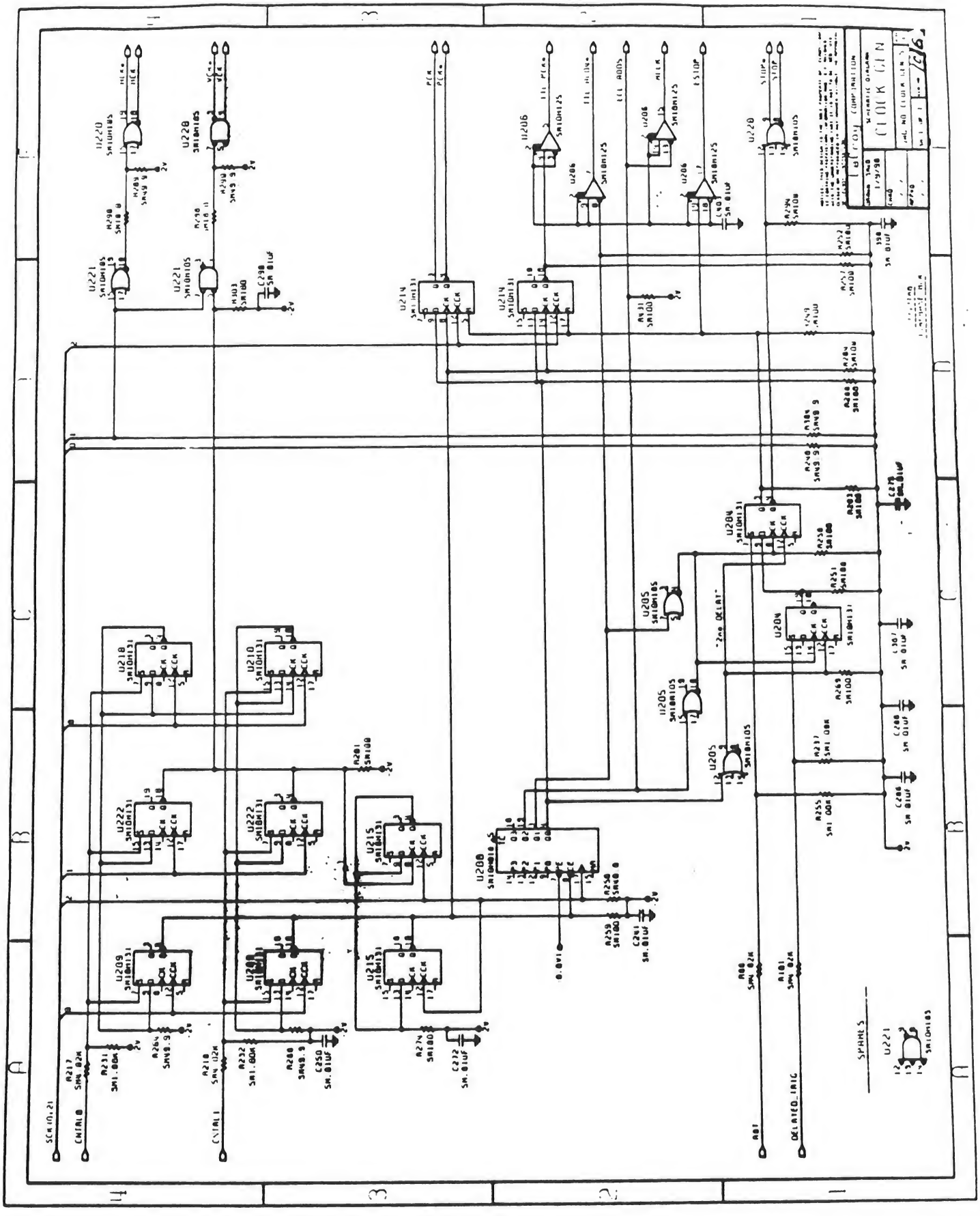

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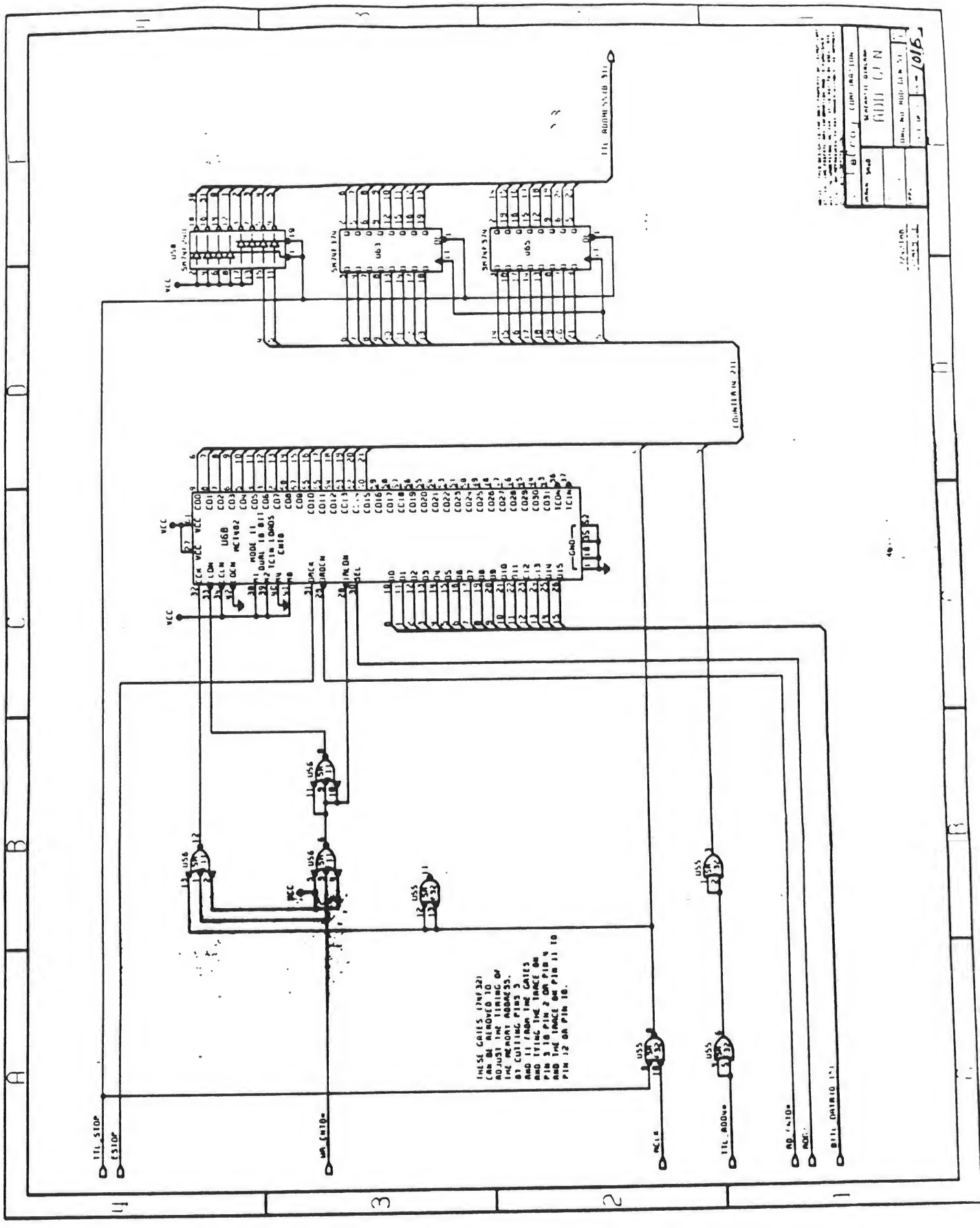
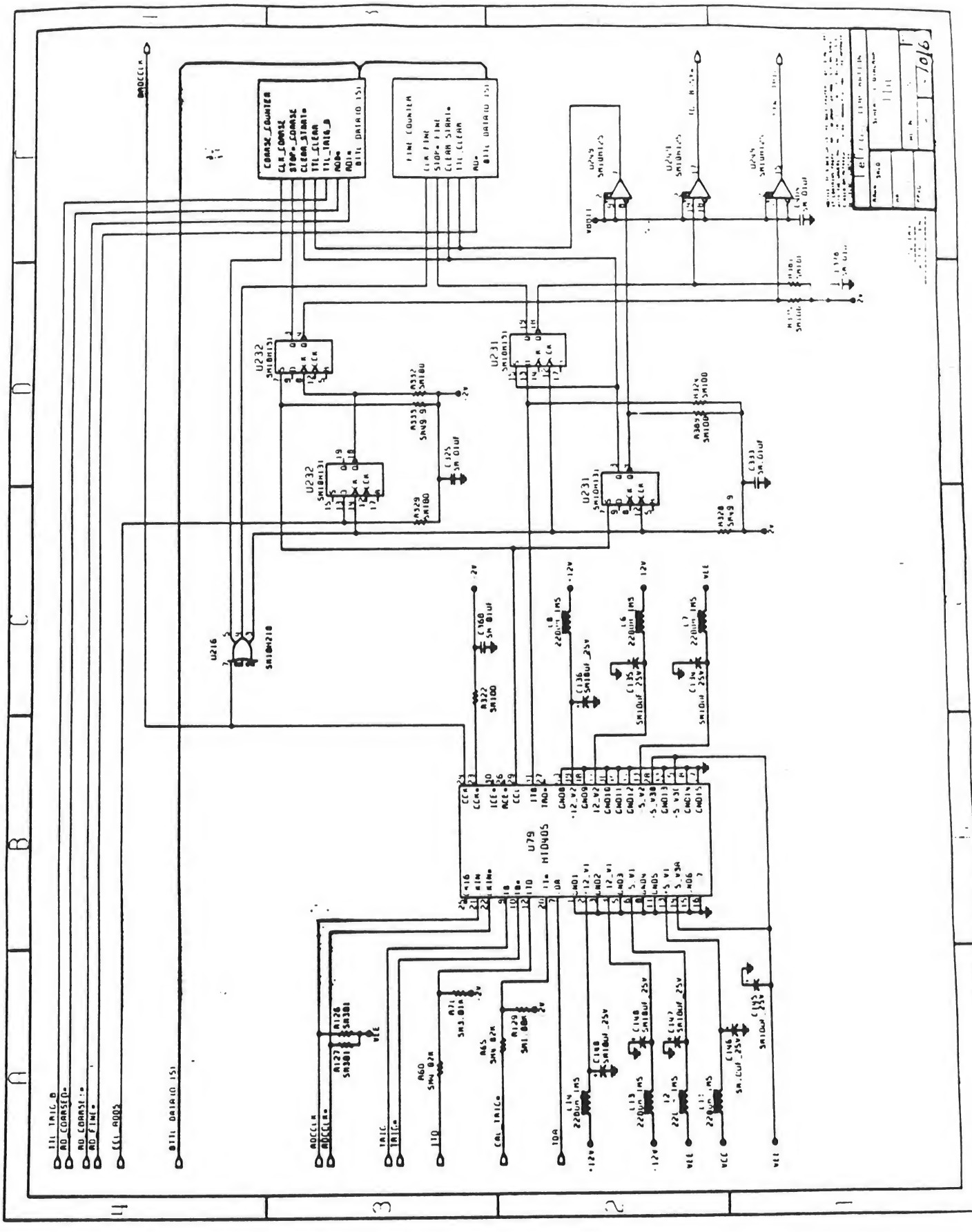
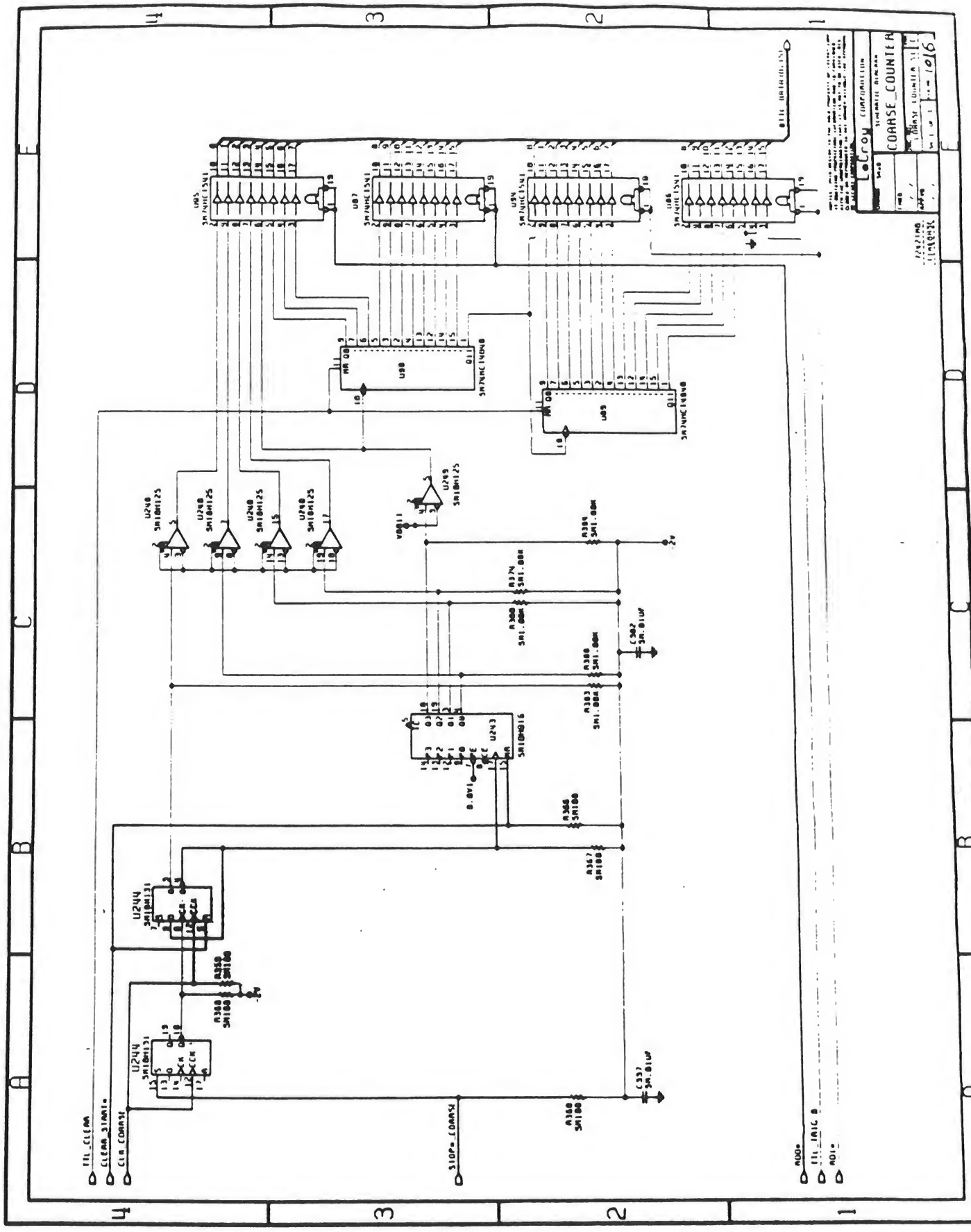


7242TMB **Sheet 7.**

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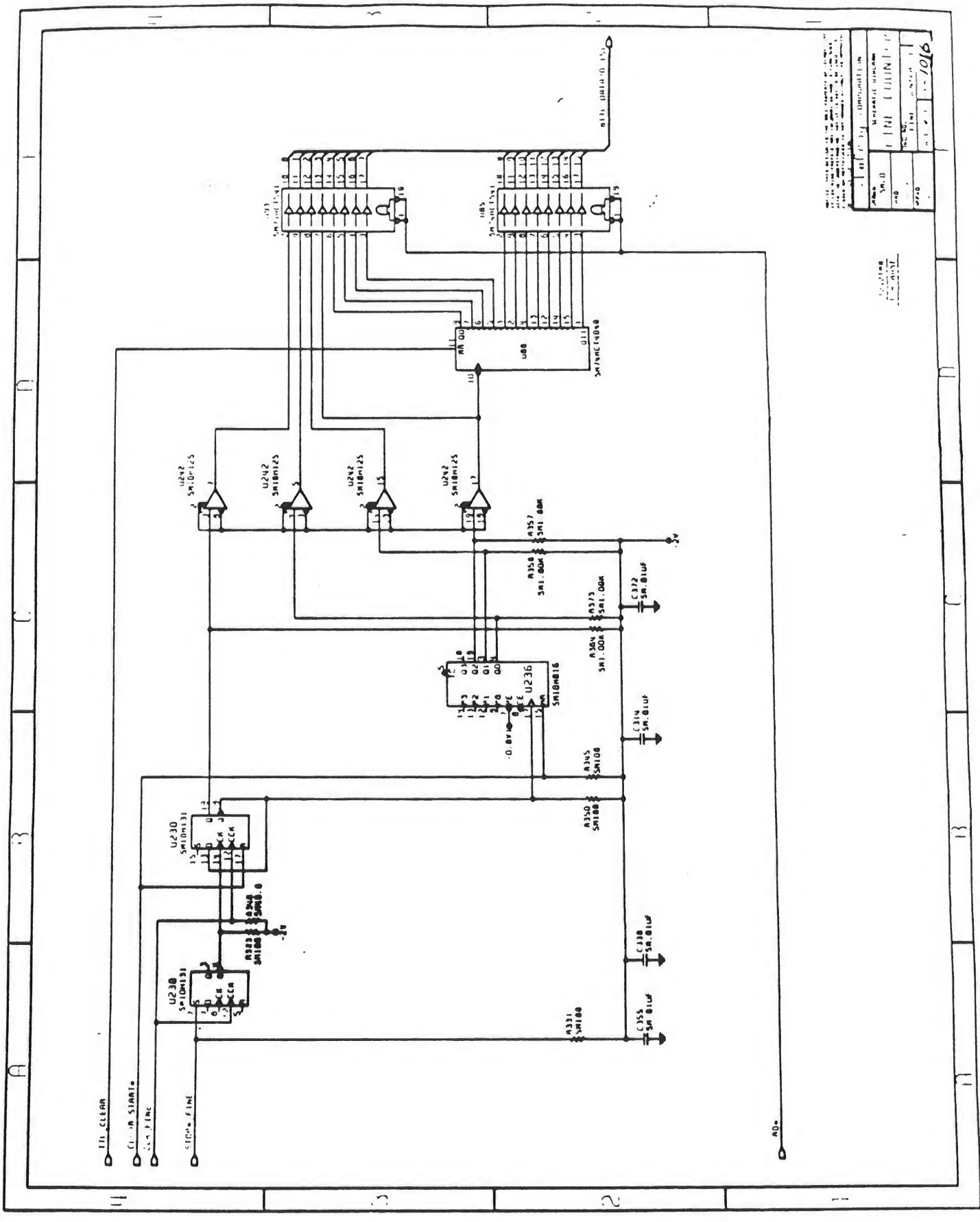
1016



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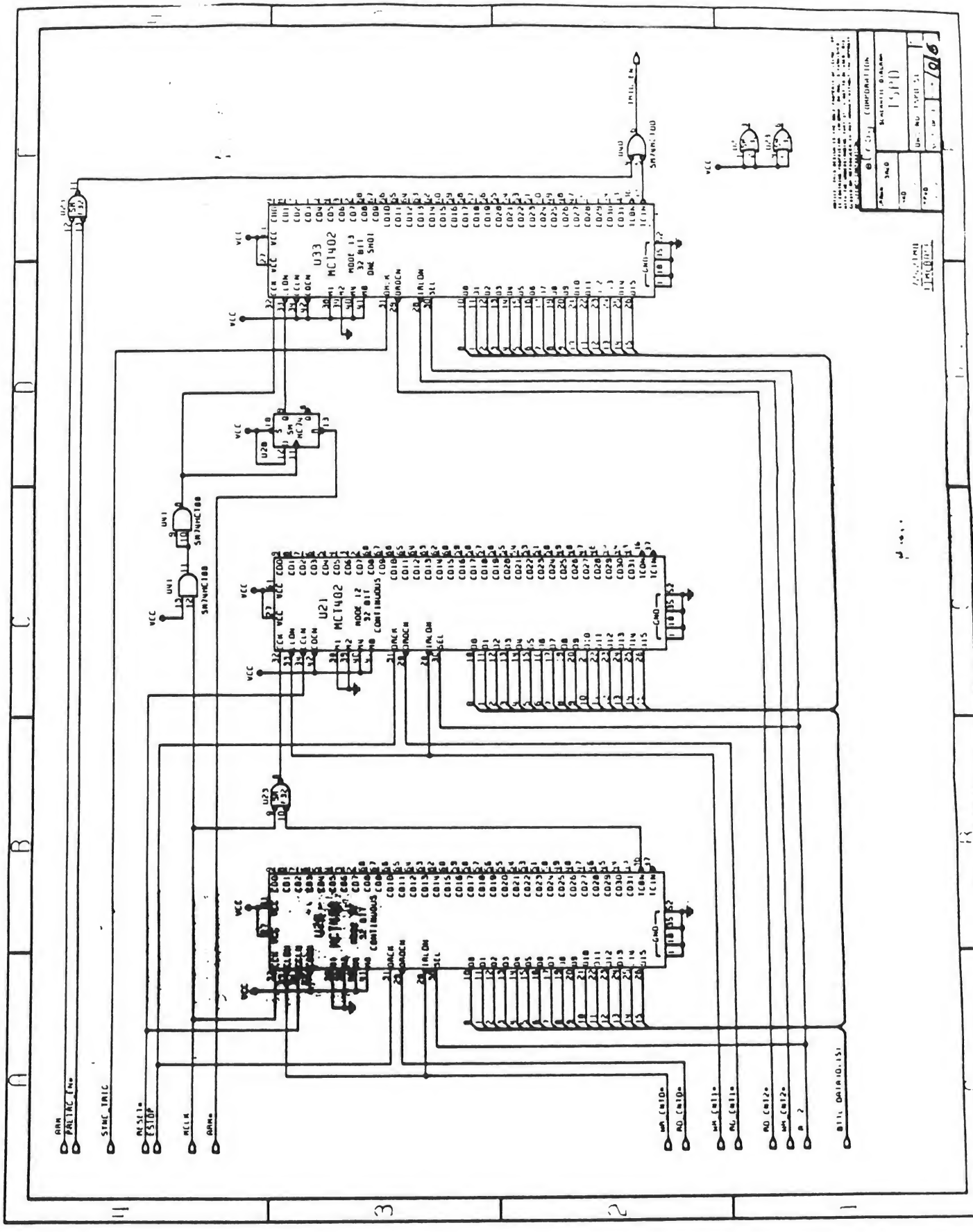

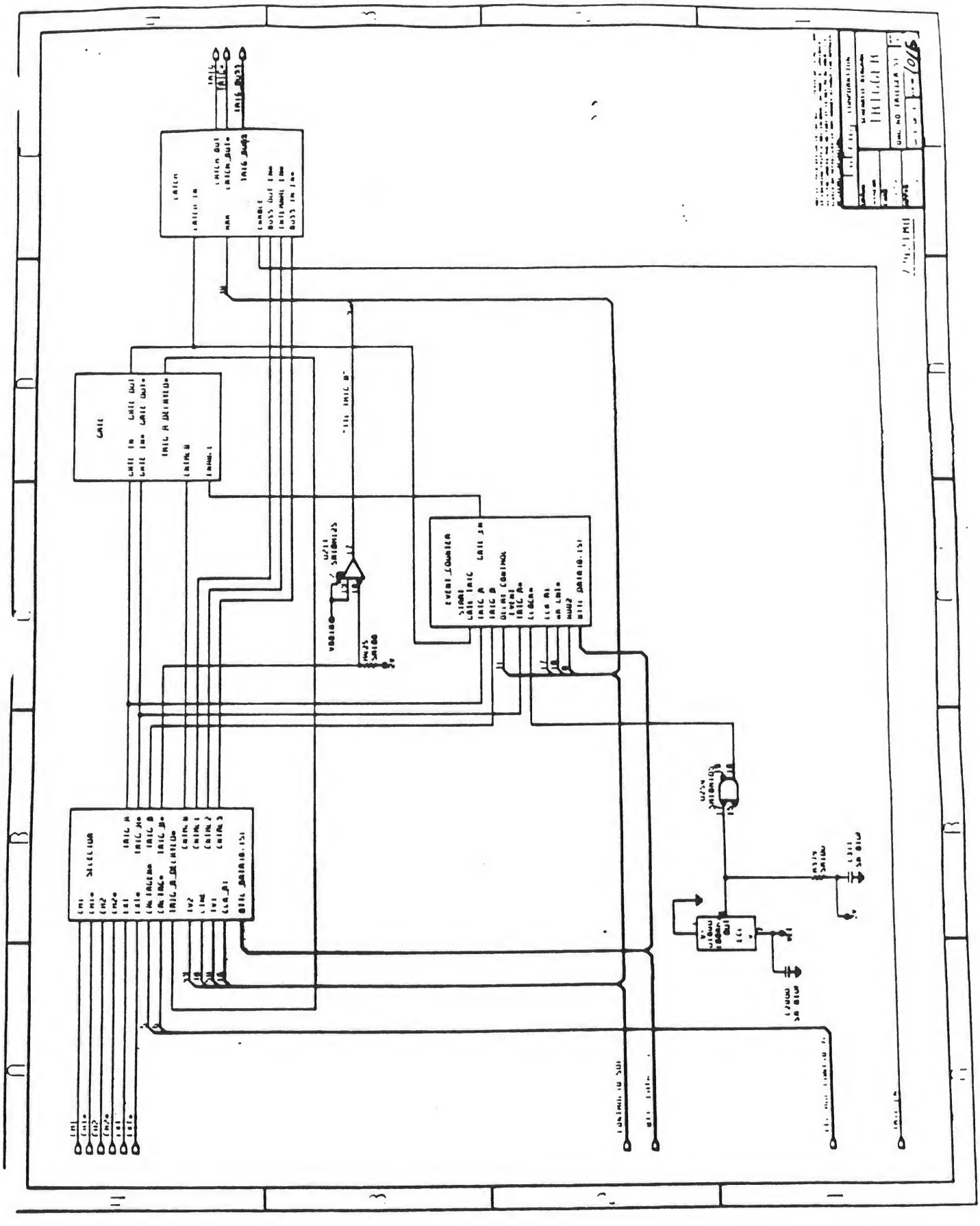

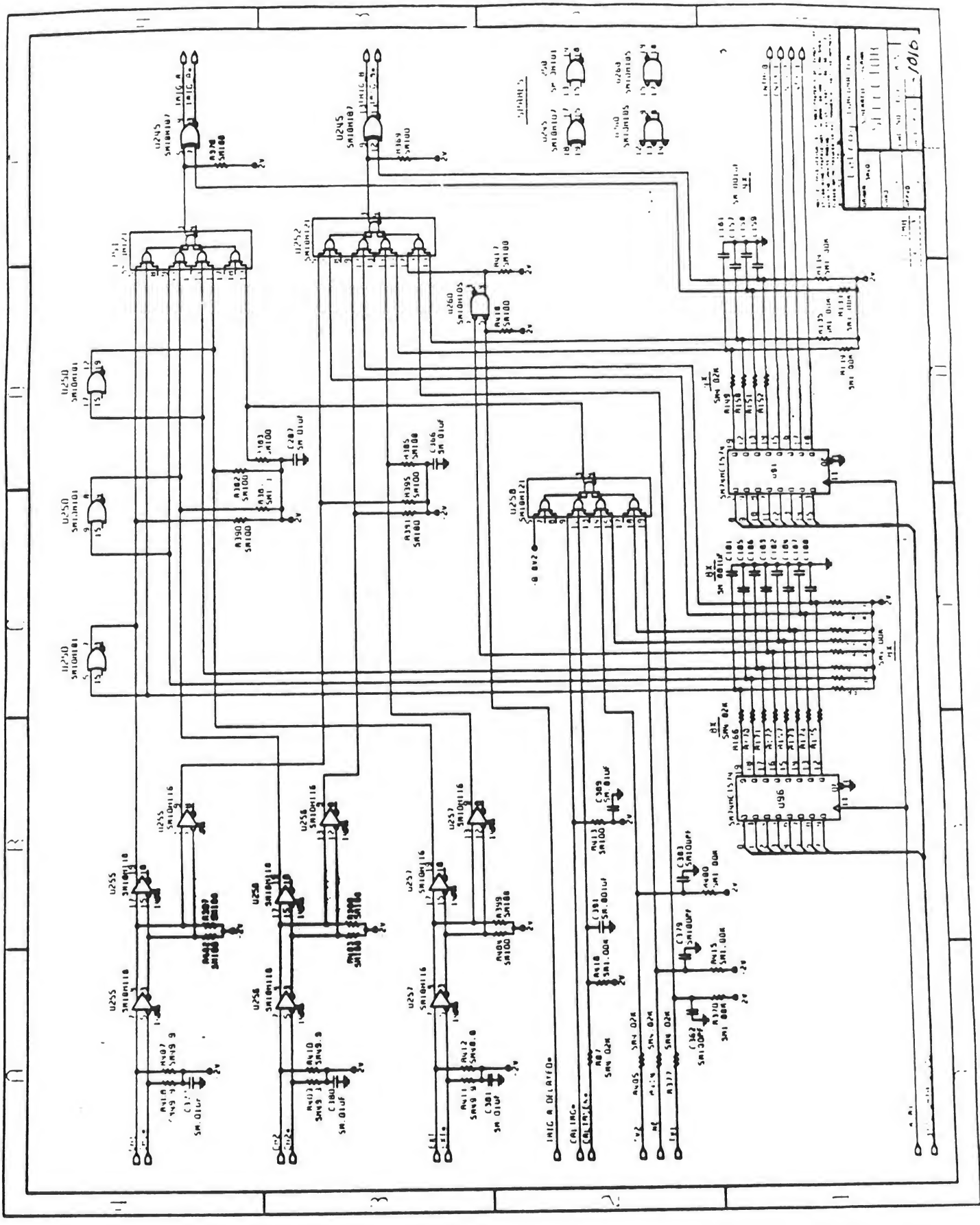

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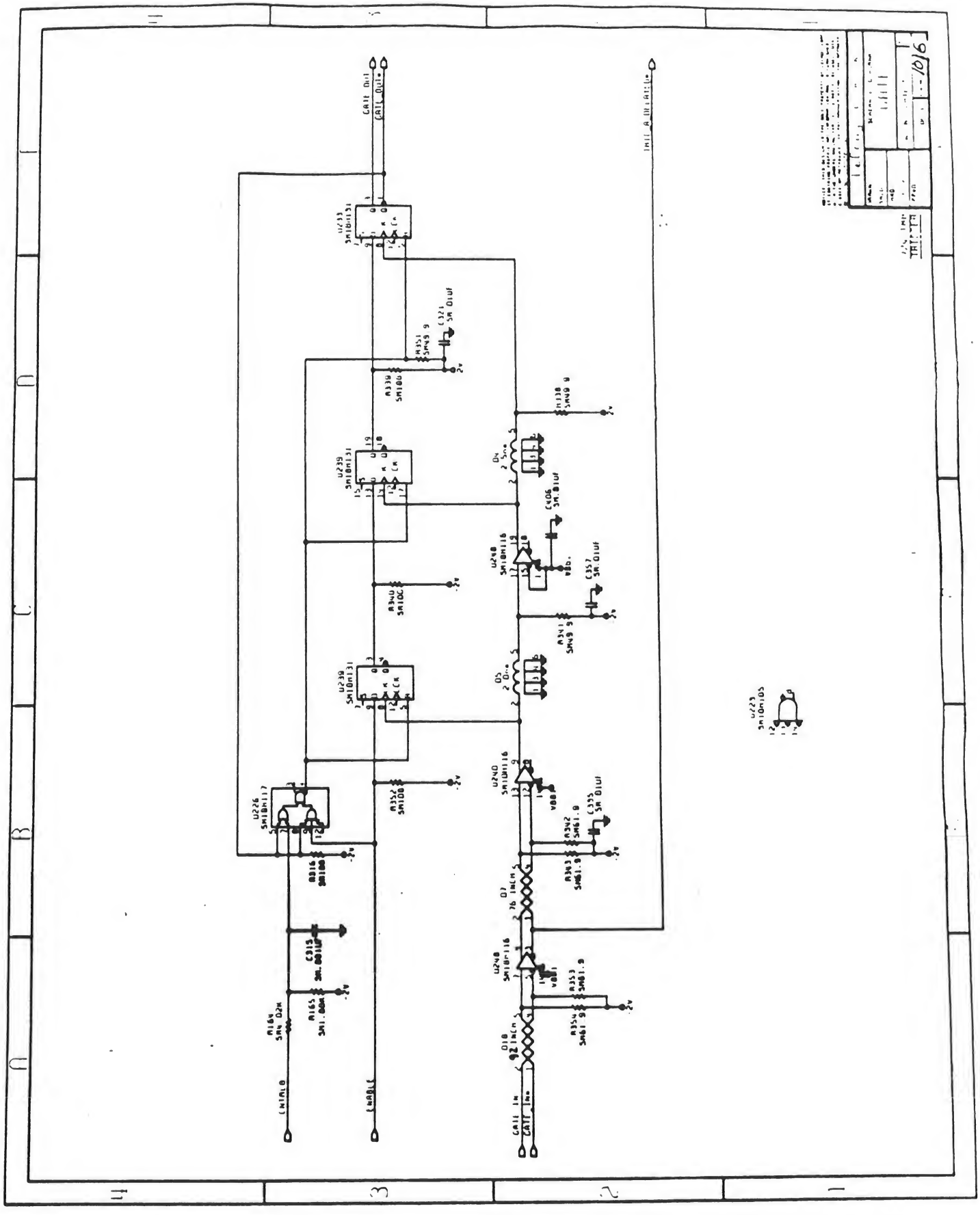

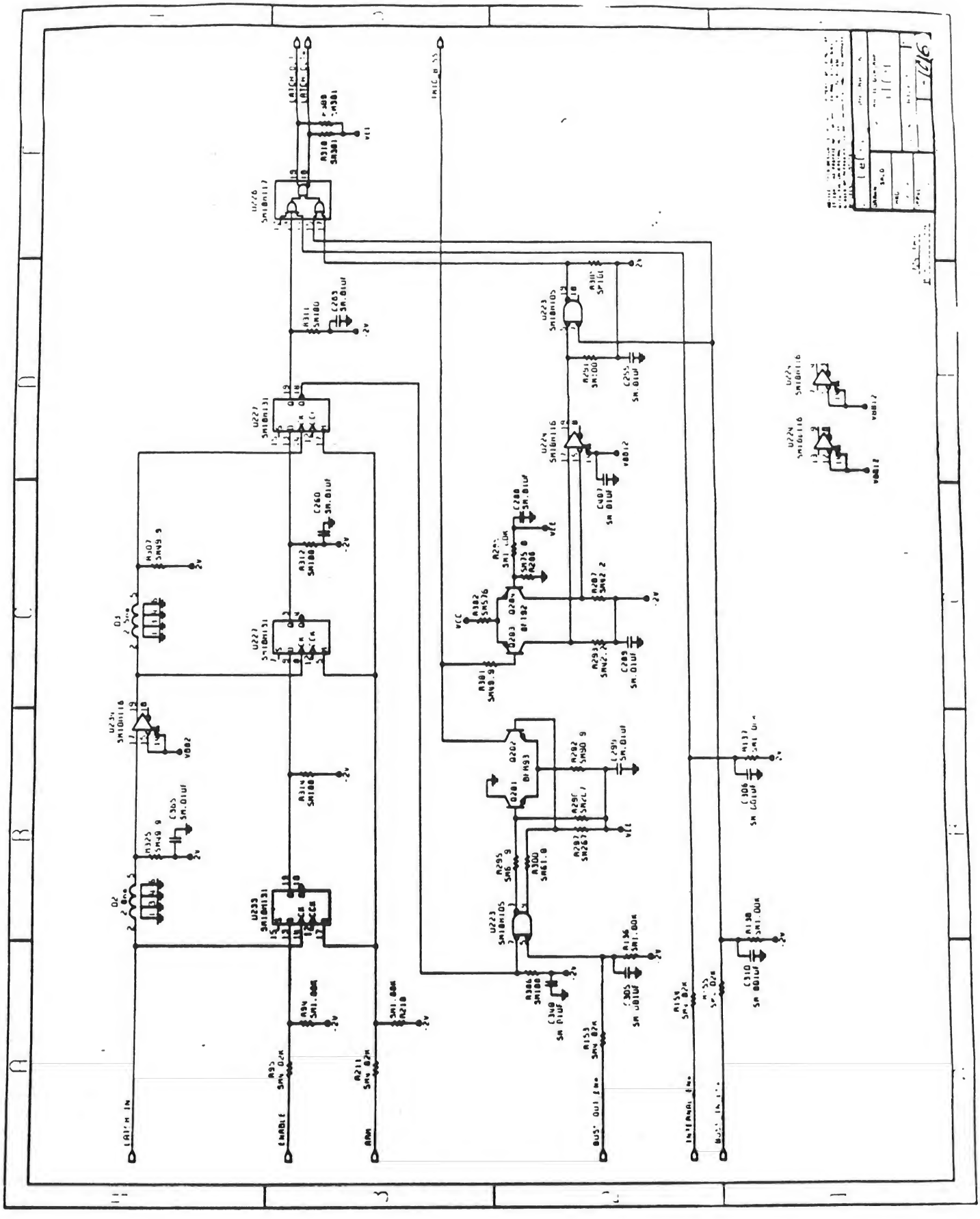

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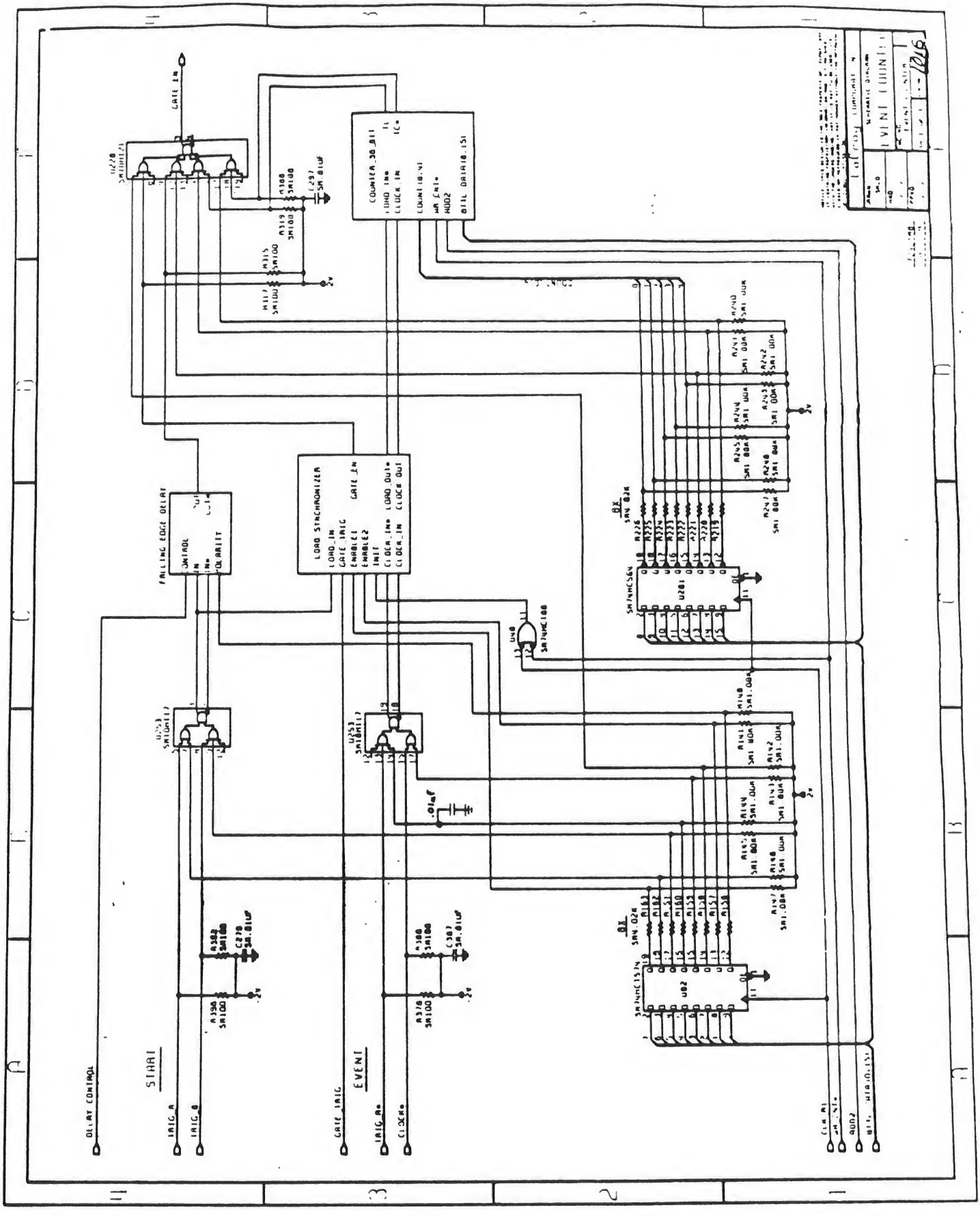

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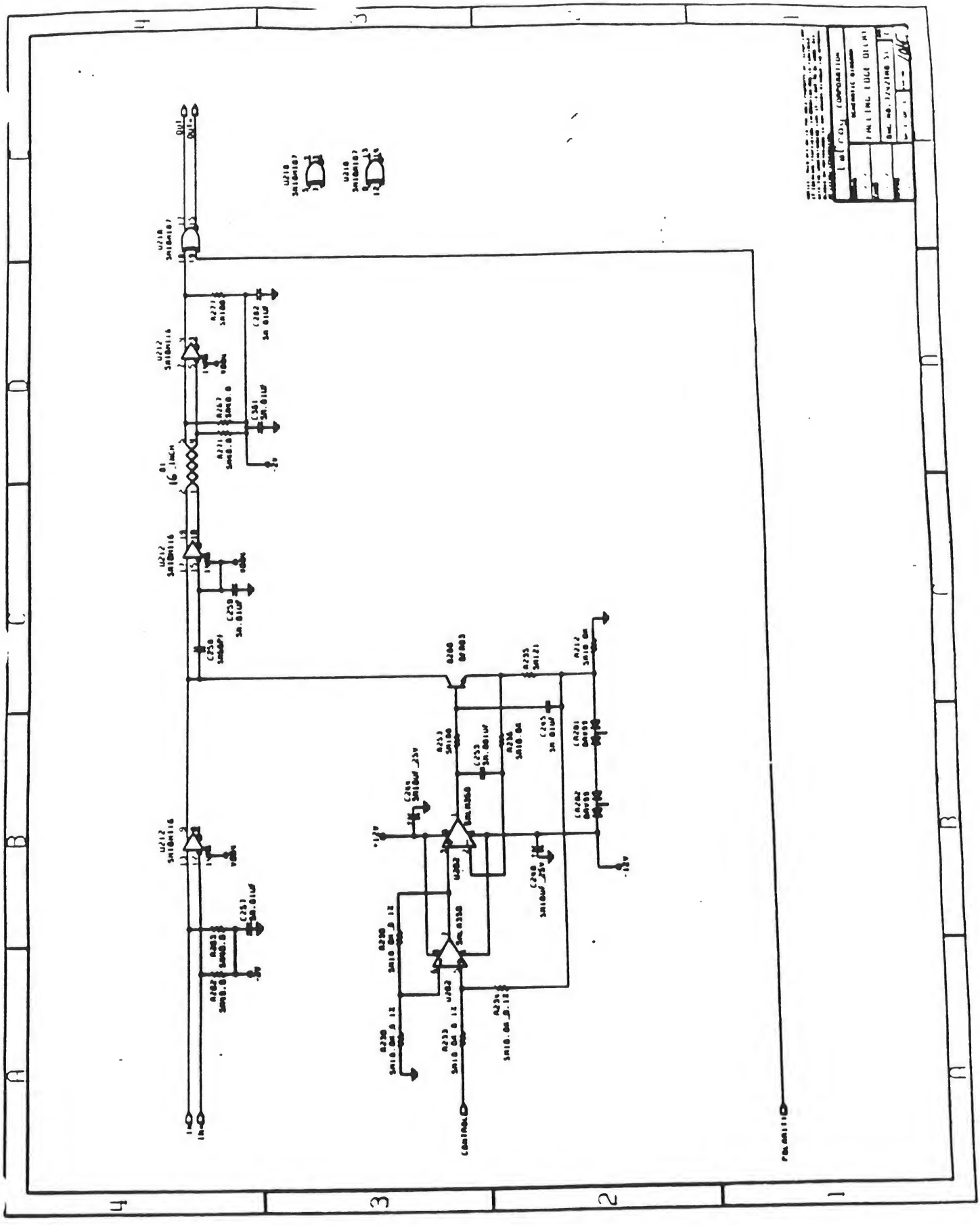

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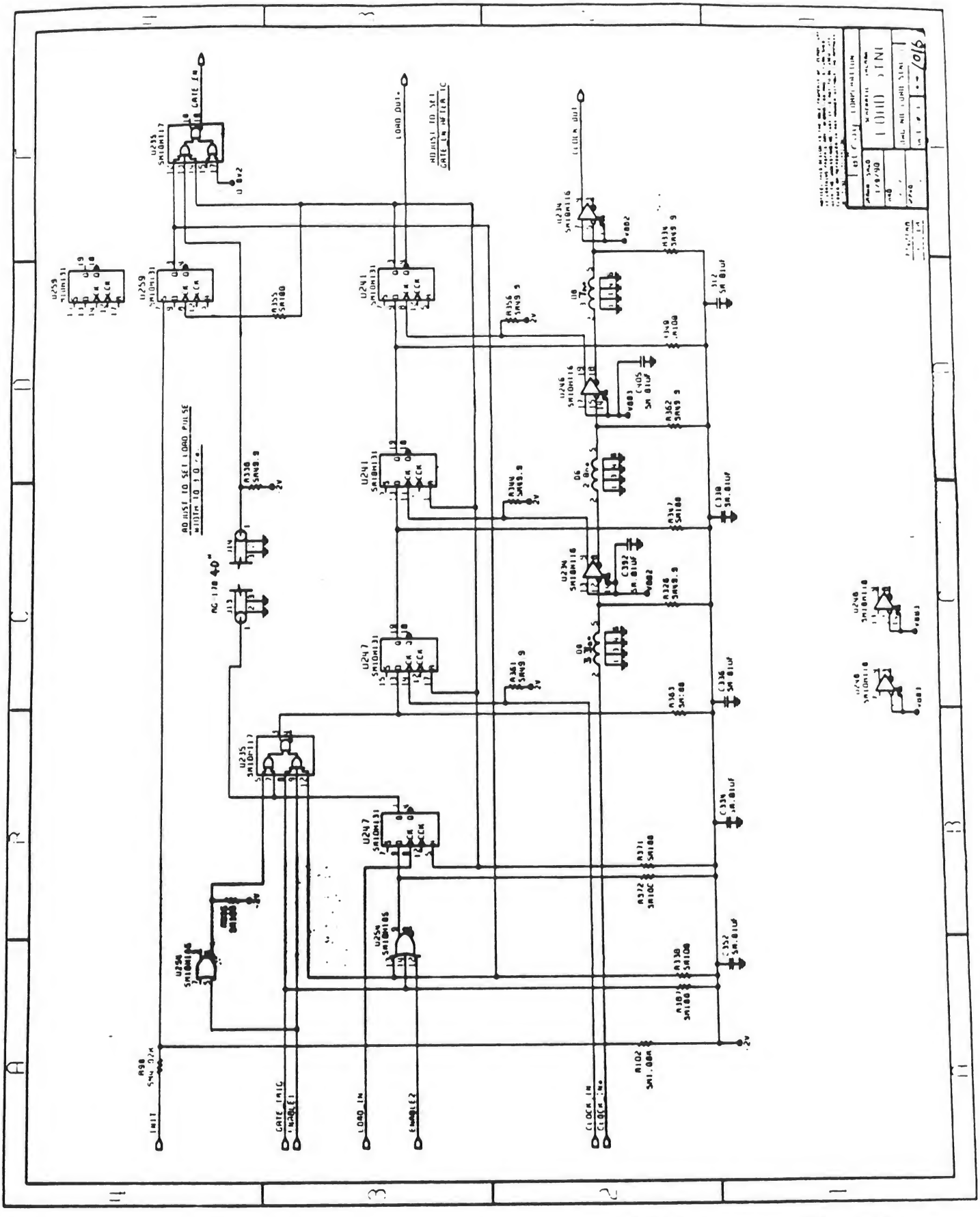

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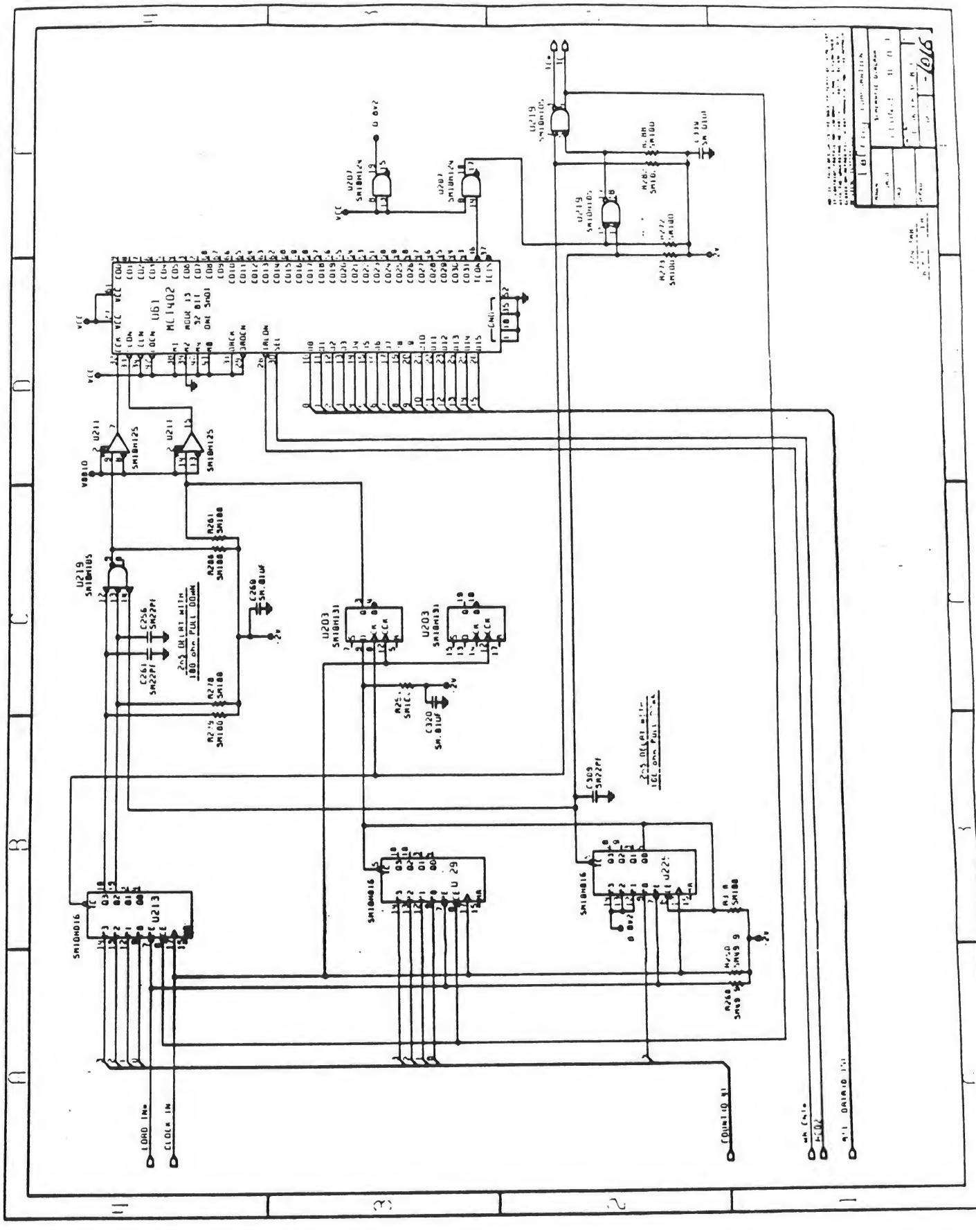

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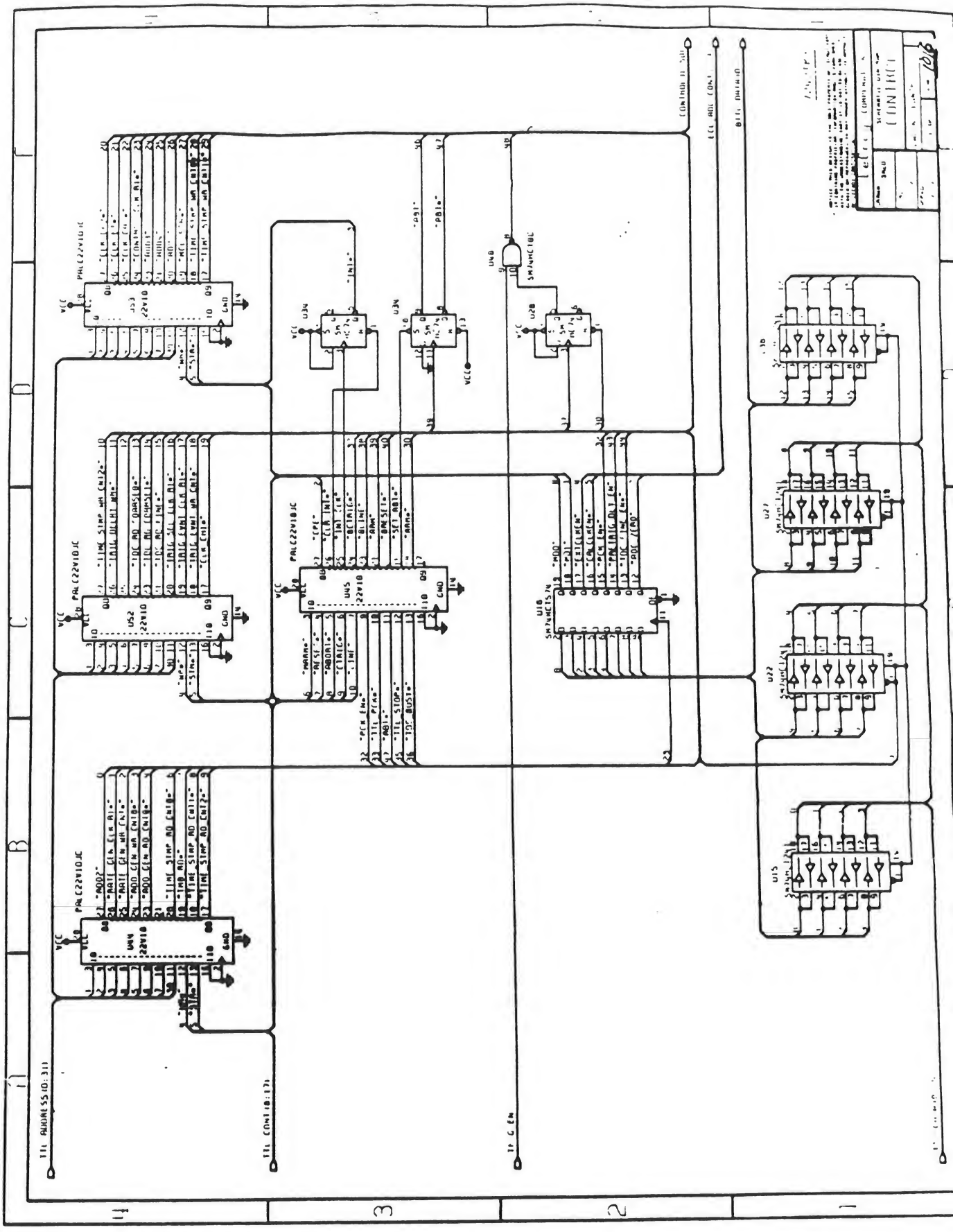

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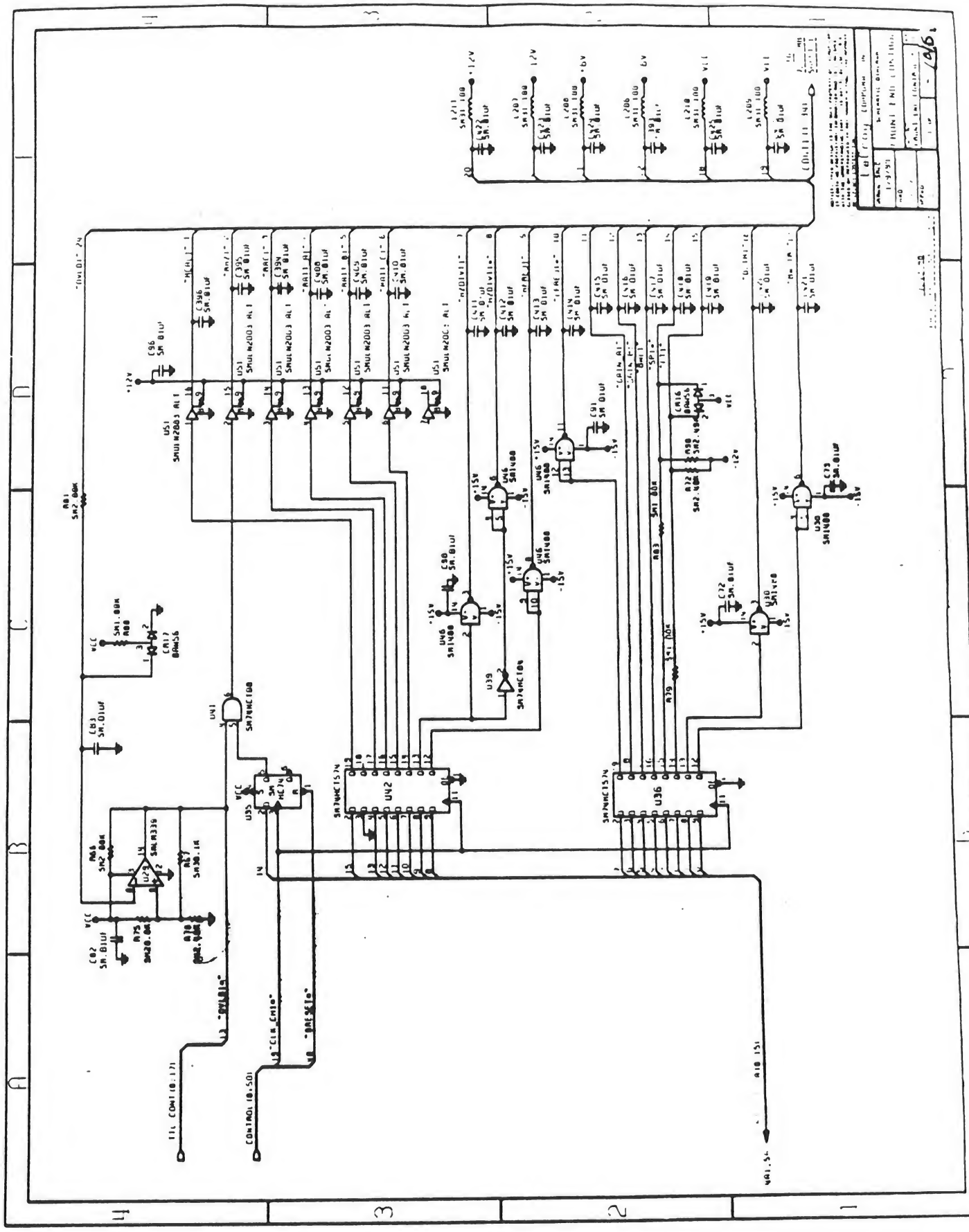

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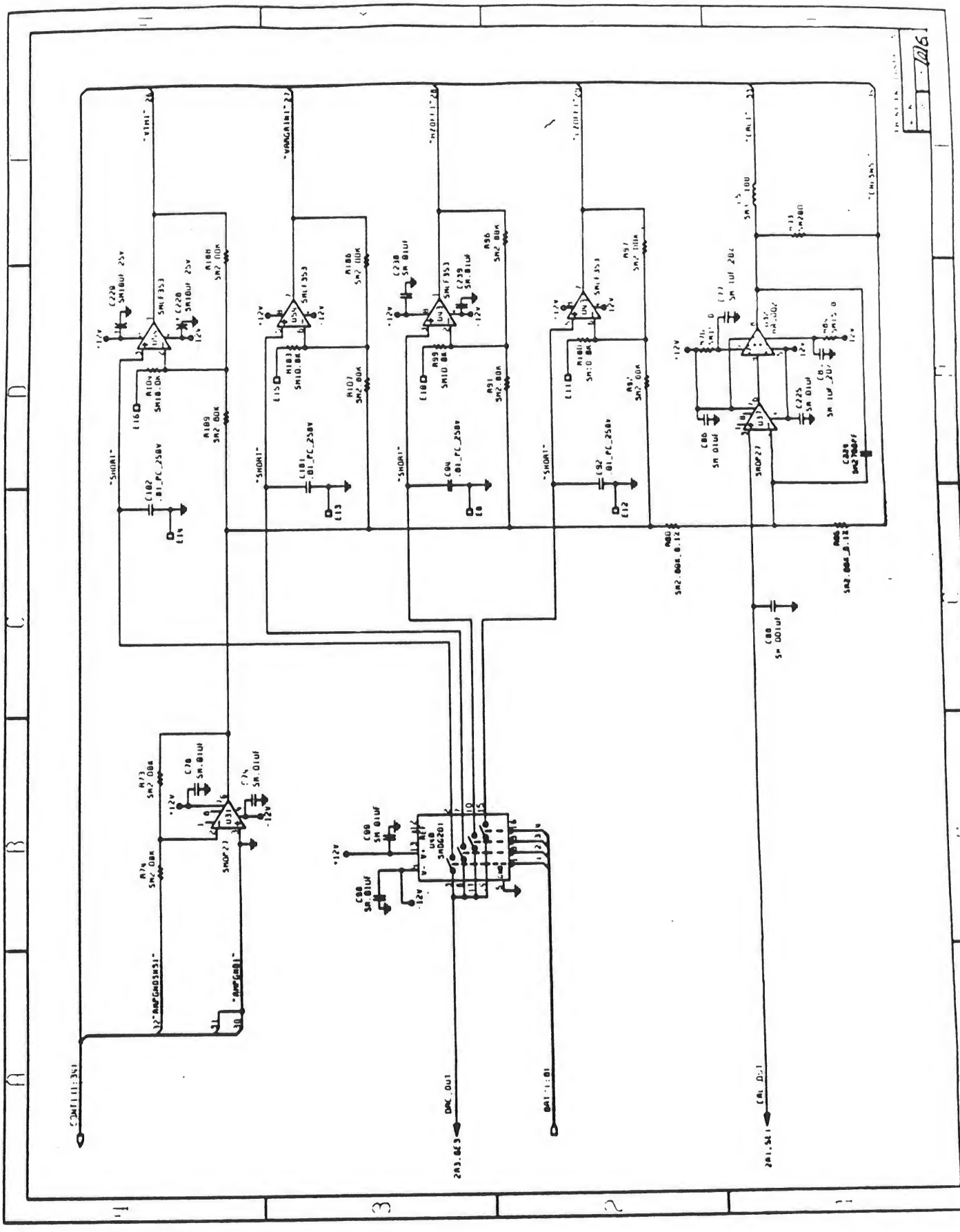

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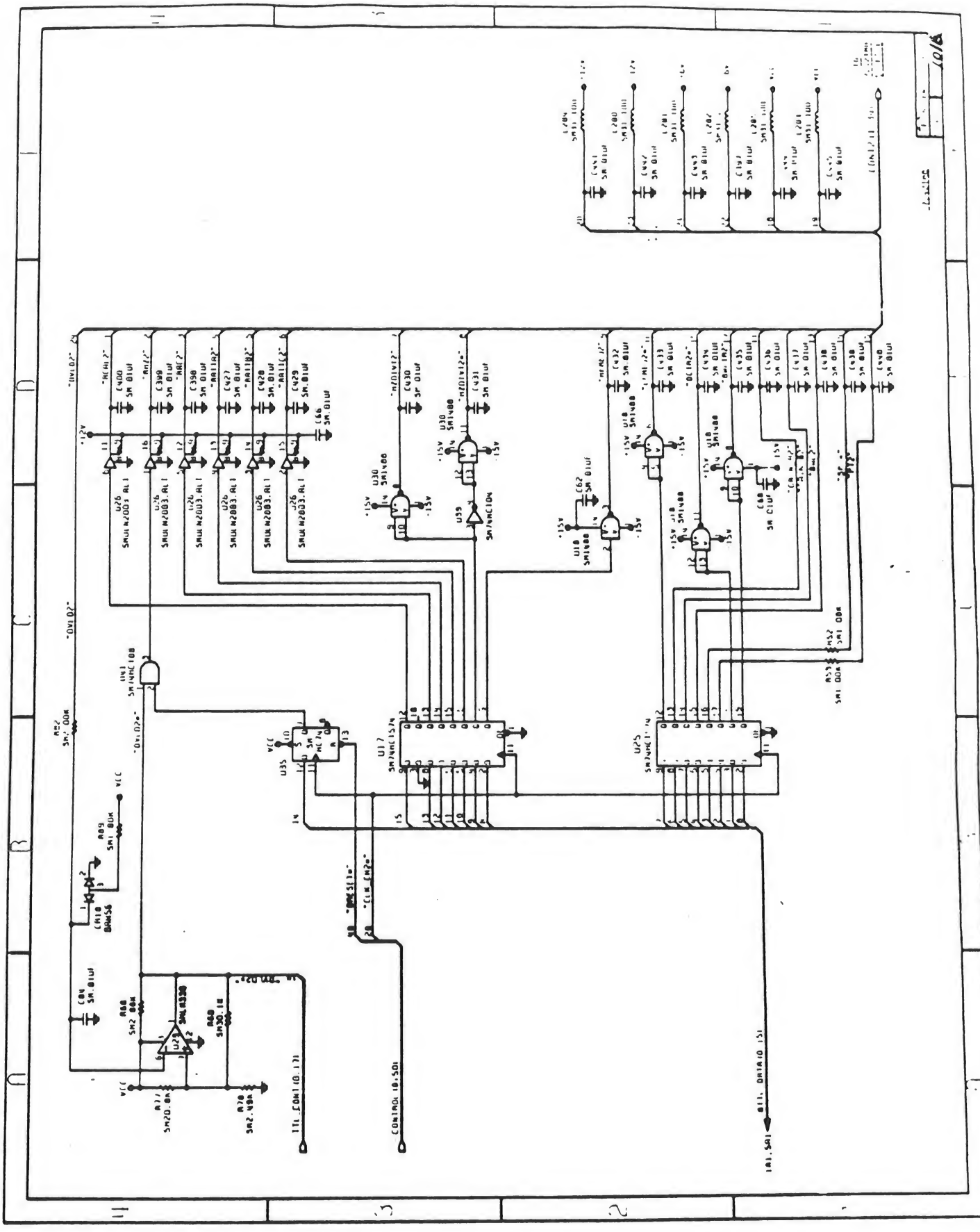

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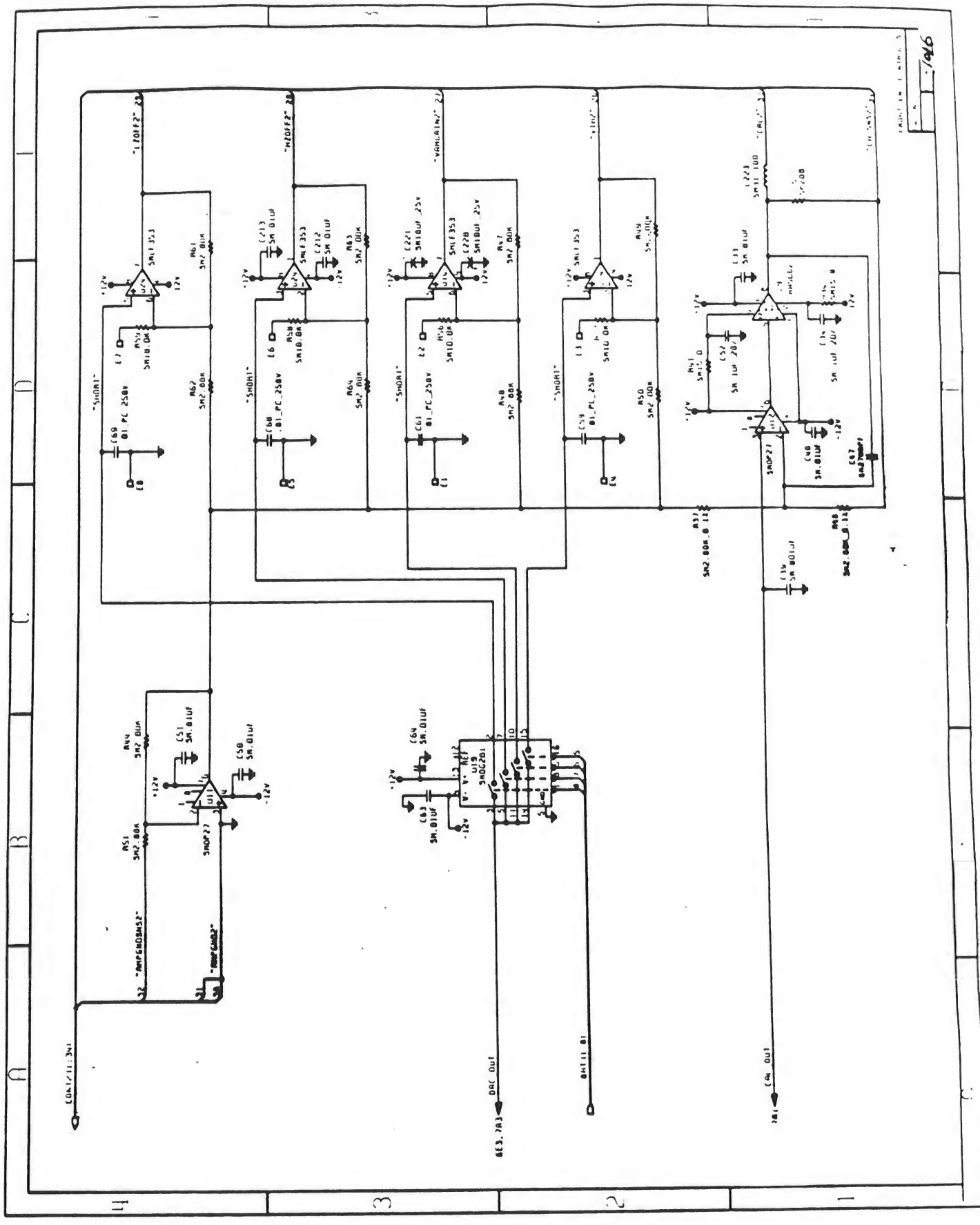

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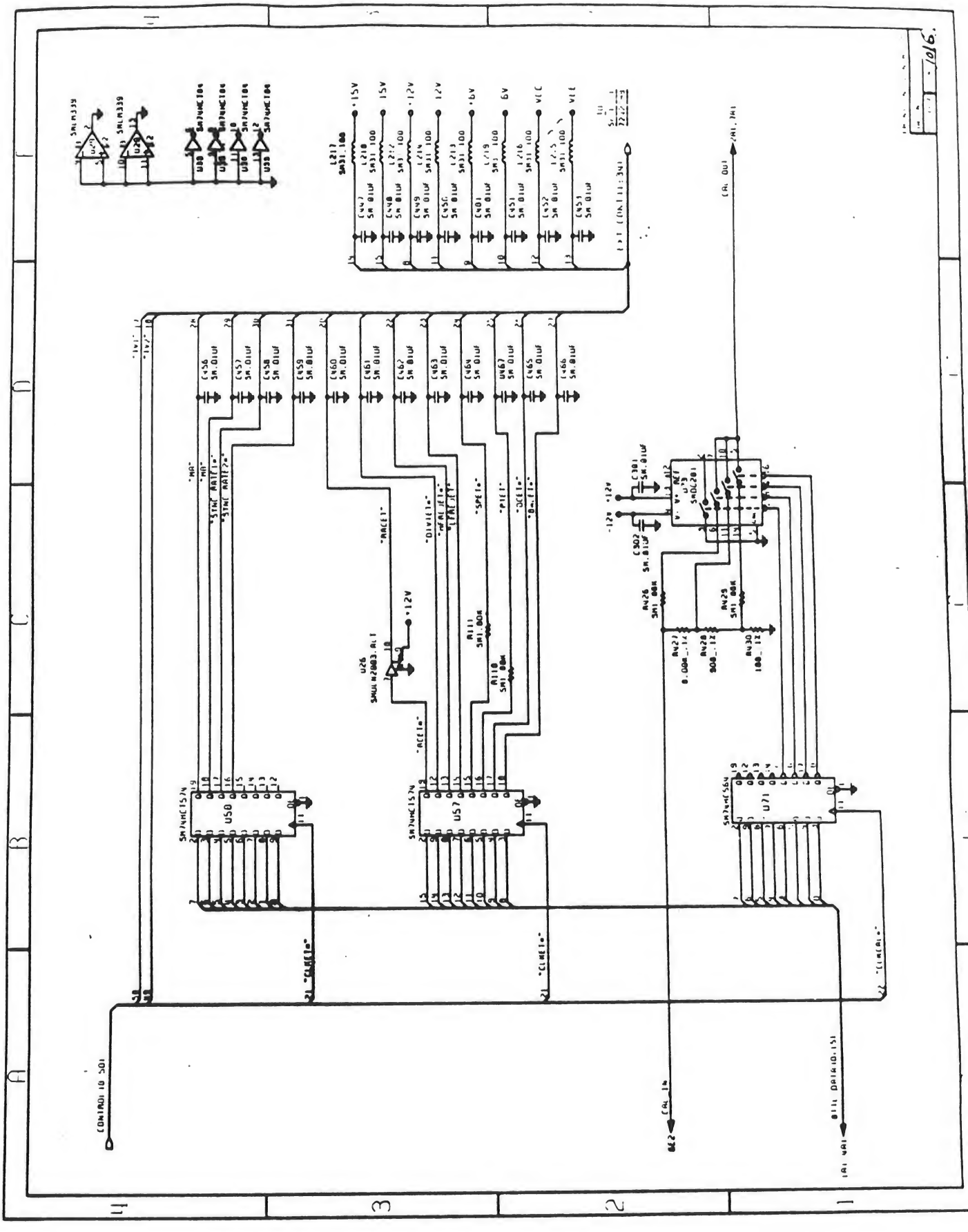

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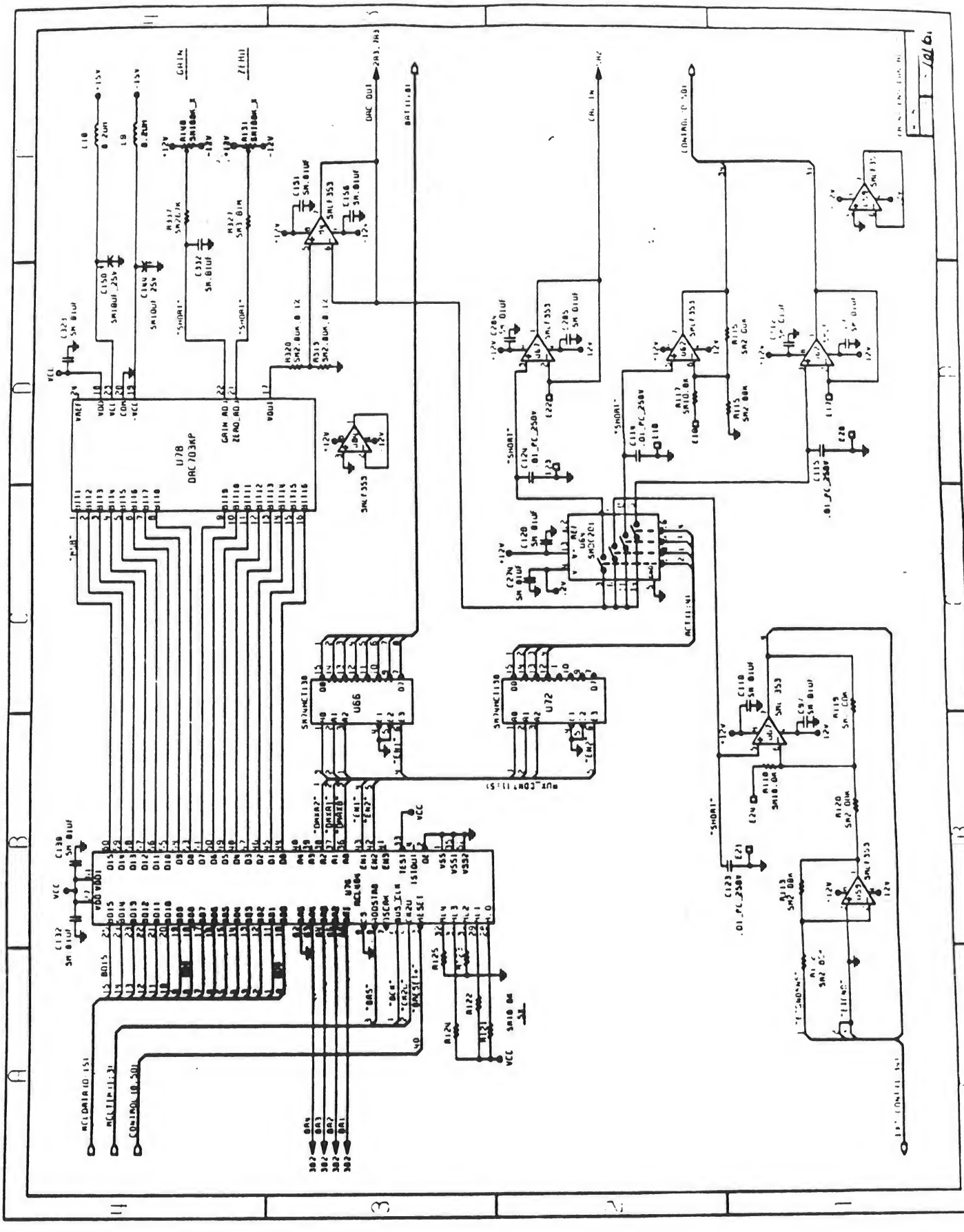

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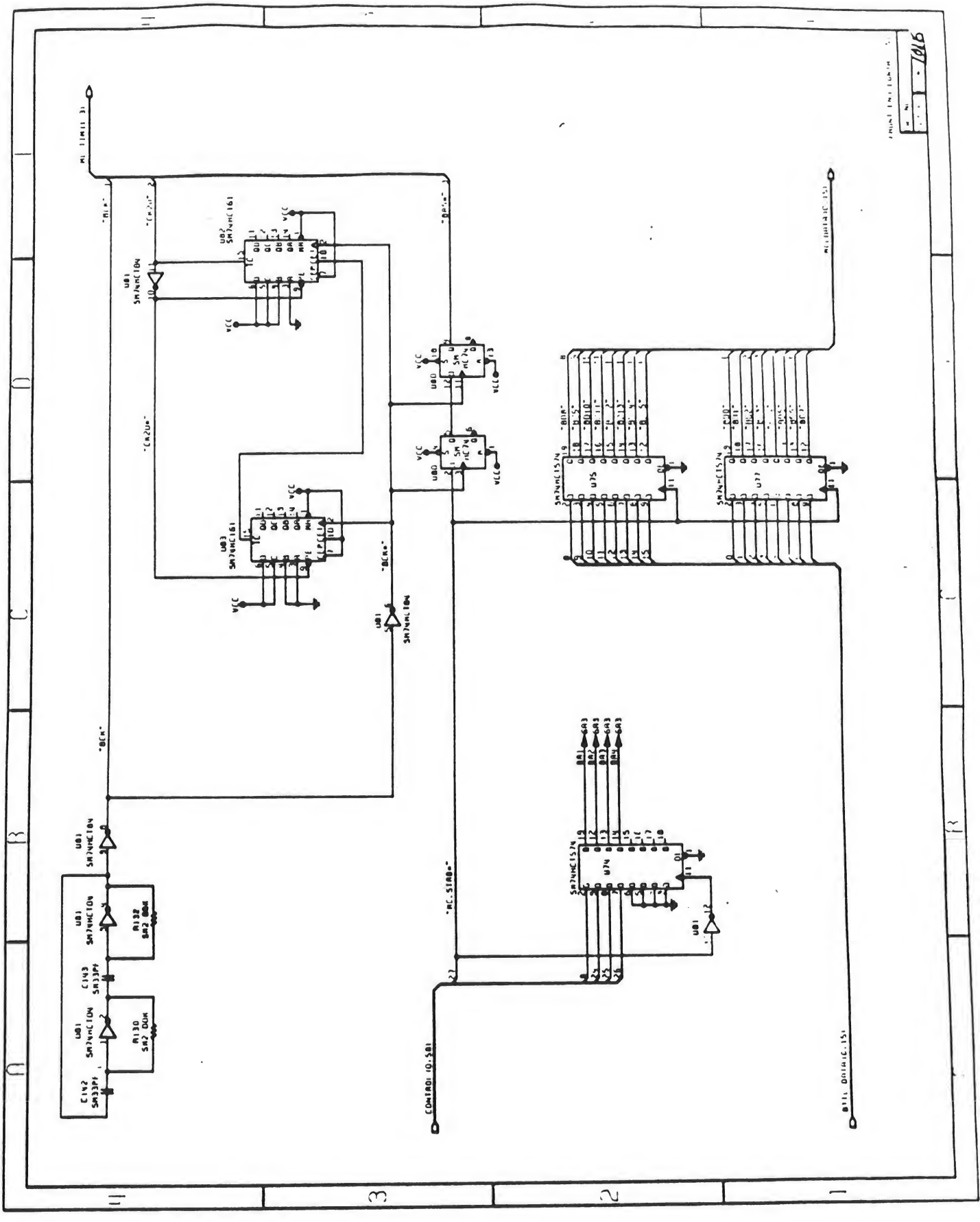
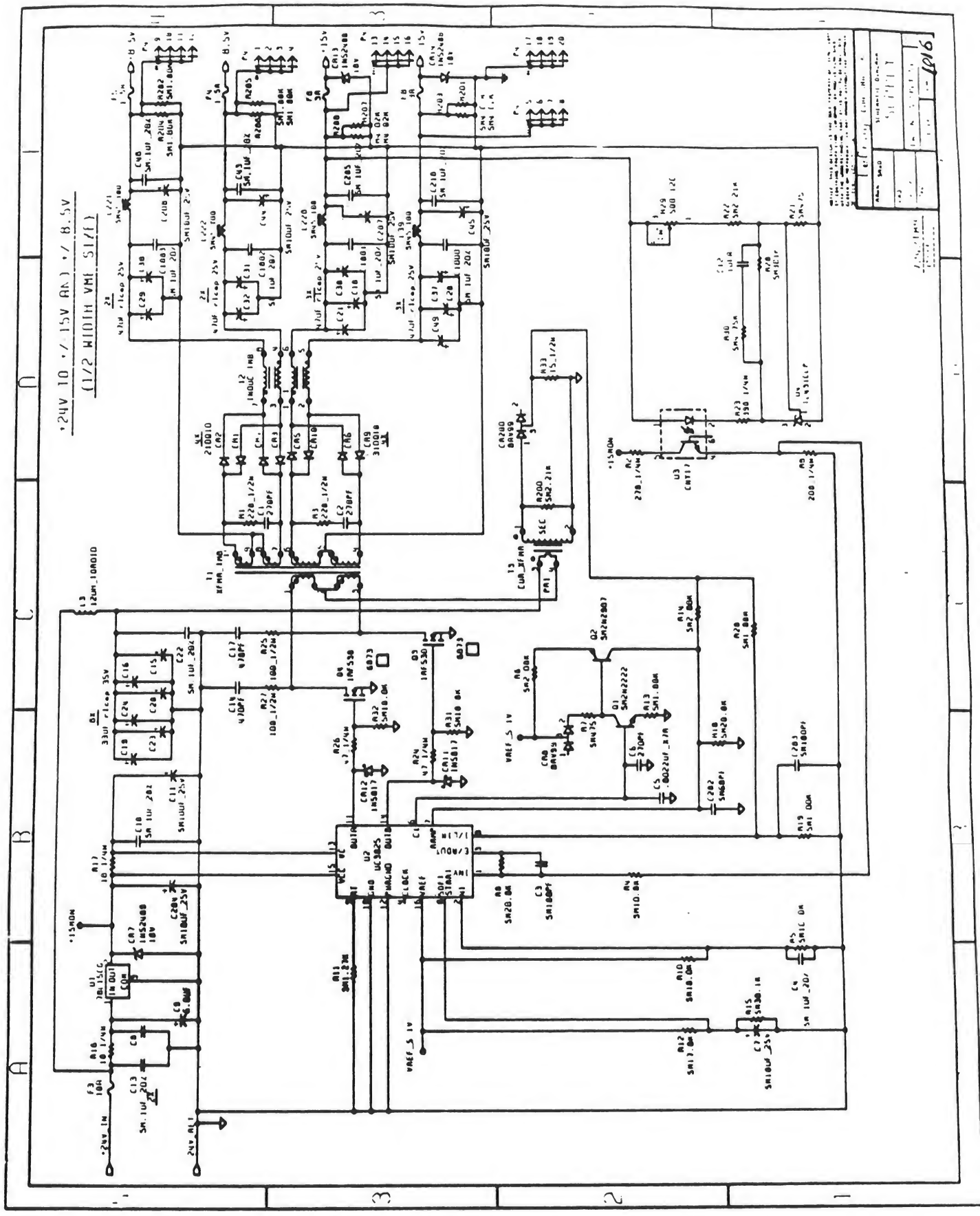


7242TMB **Sheet 27.**



7242TMB **Sheet 28.**

LECROY 7242B PLUG-IN MODULE PARTS LIST

8.0 INTRODUCTION

This section contains the parts list for the 7242B. It is divided into two categories: Replaceable Parts and Complete Parts. The Replaceable Parts list contains items that this manual will support replacing as well as the parts that will be readily available from our service centers. All of the parts on this list should be available within 24-36 hours upon request. The Complete Parts list contains the full parts list for all of the assemblies contained in the 7242B.

8.1 REPLACEABLE PARTS LIST

7242ADCA	ADC Board (replaced as a set with the 7242AMP)
7242AMP	Amplifier Assy. (replaced as a set with 7242ADCA)
7242EXTR	External Trigger Assy
7242FPCB	Front Panel Board
7242BFRNT	Front Panel Assy
7242ICON	Interconnect Board
7242BMEM	Memory Board
7242BMEMA	Memory Board with 1M Option
7242SINTF	INTF Board
7234TMB	Timebase/Trigger Board
7242TAMP	AMP to TMB Interconnect Board

8.2 COMPLETE PARTS LIST

8.2.1 7242BPLUG PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1000	377720002	LABEL U.S. FLAG "MADE IN U.S.A."	1	
	377724212	LABEL FOR 7242B-F2	1	
	530009001	SHIELD (RFI/EMI) FINGER STOCK	1	
	530009019	GROUNDING/SHIELDING CONTACT	1	
	550130106	SCREW PAN HD M3X6	3	
	550130504	SCREW FLAT HD M3X4	4	
	550130506	SCREW FLAT HD M3X6	12	
	550130508	SCREW FLAT HD PHILIPS	4	
	550430104	SCREW CYL HD PHIL M3X4	2	
	551130201	WASHER SPLIT LOCK M3	6	
	552430100	NUT HEX M3	3	
	553830105	SPACER HEX M3X5	1	
	575901002	WASHER .280ID X .375OD X .022TH	1	
	707242815	REAR BRACKET 7242	1	
	707242816	DIE-CUT INSULATOR 7242	1	
	707242817	WASHER, MYLAR	1	
	707242867	RETAINING SPRING 7242	1	
	707242875	LATCH ASSEMBLY 7242	1	
	707242876	RETAINING SCREW 7242	1	
	707242912	CLAMP 7242	2	
	707242921	RAIL 7242	1	
	707242931	HOUSING FOR 7242	1	
	7234TMB	TMB MODULE ASS'Y 7234	1	
	7242ADCA	PCB ASS'Y 7242ADC (SIEMENS)	1	
	7242AMP	AMPLIFIER ASSEMBLY 7242	1	
	7242BFRNT	FRONT PANEL ASS'Y 7242B	1	
	7242BMEM	MEM MODULE PCB ASSY 7242B	1	
	7242EXTR	EXTERNAL TRIG ASS'Y 7242	1	
	7242ICON	INTERCONNECT PCB ASS'Y 7242	1	
	7242SINTFB	INTERFACE MODULE PCB ASSY F2 OPT	1	
	7242TAMP	AMP TO TMB PCB ASSY	1	
	C7242BPLUG	CABLE ASS'Y PROBE SENSE INTF TO AMP	1	
	C7242EXTMB	CABLE ASS'Y EXTR TO TMB	1	

8.2.2 7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	106433271	CAP CERA MONO 270PF	1	C12
	106433471	CAP CERA MONO 470PF	2	C14, C15
	106433561	CAP CERA MONO 560PF	2	C7, C8
	106435103	CAP CERA MONO .01UF	6	C47, C49, C51, C53, C56, C58
	106435473	CAP CERA MONO .047UF	1	C16
	106445222	CAP CERA MONO 2200PF	1	C11
	141264476	CAP TANT DIP 10V 47 UF	1	C31
	141854685	CAP TANT DIP 6.8 UF	44	C9, C13, C40-C45, C48, C50, C52, C55, C57, C59, C61-C65, C67, C69, C91, C71-C77, C98, C361, C353-C355, C362, C365, C369, C372-C375, C379, C46, C54
	142824685	CAP TANT DIP CASE 6.8 UF	2	C376, C377
	146474337	CAP MINI ALUM 20% 330 UF	4	C17-C20
	146674157	CAP MINI ALUM 20% 150 UF	4	C1-C4
	146674336	CAP MINI ALUM 20% 33 UF	3	C68, C70, C335
	158849011	CAP VARIABLE 2.5 - 10 PF	1	C356
	161335100	RES CARBON FILM 10 OHMS	2	R8, R11
	161335201	RES CARBON FILM 200 OHMS	1	R33
	161335271	RES CARBON FILM 270 OHMS	1	R32
	161335470	RES CARBON FILM 47 OHMS	2	R9, R10
	161335621	RES CARBON FILM 620 OHMS	1	R405
	161335680	RES CARBON FILM 68 OHMS	1	R31
	161445150	RES CARBON FILM 15 OHMS	1	R42

7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	161445151	RES CARBON FILM 150 OHMS	16	R146, R146A, R166, R166A, R200, R200A, R232, R232A, R322, R322A, R341, R341A, R374, R374A, R394, R394A
	161445510	RES CARBON FILM 51 OHMS	2	R1, R2
	161555121	RES COMP 1W 5% 120 OHMS	2	R6, R7
	180247102	RES VARI CERMET 1 K	1	R34
	200131040	IC PHASE-FREQ DET MC12040	1	U67
	200442009	IC 2 MOD PRESCALER MC12009P	1	U66
	200444016	IC BINARY COUNTER 10H016	1	U64
	208110027	IC OP AMP OP27EP	1	U65
	208122337	IC ADJ -VOLT REG LM337T	2	VR1,VR2
	208164002	IC VOLT REG POS MC78L15CG	1	VR5
	208510317	IC ADJ +V REG 317LZ	2	VR6,VR8
	208570317	IC ADJ +V REG LM317	3	VR3,VR4,VR7
	208590336	IC VOLT REFERENCE LM336	2	CR13, CR17
	208590337	IC VOLT REG NEG ADJ LM337	1	VR9
	208590431	IC ADJ SHUNT REG TL431	1	CR8
	208591385	IC VOLT REF ADJUST 385	2	CR14, CR20
	208617662	IC VOLT CONVERTER 7662CPA	1	U59
	208650393	IC DUAL VOLT COMP LM393N	1	U68
	208743825	IC PWM CONTROLLER 3825	1	U1
	235782045	DIODE DUAL RECTIFIER MBR2045CT	2, CR6, CR7	

7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	240513248	DIODE ZENER 18V 5% 1N5248B	1	CR4
	253050817	DIODE HOT CARRIER 1N5817	2	CR2, CR3
	260022017	OPTICAL ISOLATOR CNY17-II	1	U2
	280170104	TRANSISTOR FET N VN0104N3	5	Q5, Q30, Q31, Q35, Q45
	280190530	TRANSISTOR FET "N" IRF530	2	Q1, Q2
	281170104	TRANSISTOR FET P VP0104N3	3	Q36, Q41, Q43
	290113002	DELAY LINE 0-2 N-SEC ADJUSTABLE	4	VARDLY1-VARDLY4
	290199004	DELAY LINE .4 NS	1	DLY4
	290199026	DELAY LINE 2.6 NS	1	DLY2
	290199032	DELAY LINE 3.2 NS	1	DLY1
	290199047	DELAY LINE 4.7 NS	1	DLY6
	290199049	DELAY LINE 4.9 NS	1	DLY5
	300050002	CHOKE FERRITE SINGLE LEAD	3	L2-L4
	301016104	INDUCTOR MOLDED 100 UH	2	L11, L14
	301016222	INDUCTOR MOLDED 2.20 UH	1	L12
	301377124	INDUCTOR PWR 120 UH	3	L6, L15, L19
	301377303	INDUCTOR PWR 30 UH	1	L7
	301486224	INDUCTOR SHIELDED 220 UH	6	L5, L8, L9, L16, L17, L18
	302382120	INDUCTOR WOUND 12 UH	1	L1
	308088040	OSCILLATOR VOLT CONTR 400-600 MHZ	1	U63
	309040015	CRYSTAL OSCILLATOR 15.5642 MHZ	1	U25
	377041055	LABEL "7242ADCA"	1	
	402610003	CONN CO-AX PC MTG SMB	5	J1-J5
	405764122	SOCKET SINGLE WIRE 22-POS	6	U3, U16
	430542732	RELAY FORM C DPDT 732-2A20	1	K1

7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	433220001	FUSE PICO II 125V 10 AMP	2	F2, F8
	433220003	FUSE PICO II 125V .5 AMP	1	F1
	433221004	FUSE PICO II 125V 1 AMP	2	F6, F7
	433222005	FUSE PICO II 125V 2 AMP	3	F3, F4, F5
	440202101	TRANSFORMER 7242ADC-T1	2	T2,T3
	440242403	TRANSFORMER 7242MEM-T3	1	L20
	440282001	TRANSFORMER 72XXCT-T1	1	T1
	454420032	HDR SOLD TAIL/FEM 32	1	S01-S12
	454610048	HDR SOLD TAIL/MALE 48	1	P14
	454612096	HDR SOLD TAIL/MALE 96	3	P24, P34, P44
	500070005	MOUNTING KIT FOR TO-8	1	U63
	500120002	TRANSIPAD "LARGE"	1	
	500460006	INSULATOR THERMALFILM	6	
	500510005	INSULATOR MICA FOR 10-PIN	1	M01
	500860302	INSULATOR FOR TO-220	3	
	505051004	HEAT SINK FOR SCR CASE	2	H4,H5
	505051005	HEAT SINK FOR TO-220	2	H1,H3
	505051006	HEAT SINK DUAL FOR TO-220	2	H7,H8
	520000510	STANDOFF GLASS 8MM	4	
	550125120	SCREW PAN HD PHIL M2.5X20	1	
	550130114	SCREW PAN HD M3X14	4	
	550425114	SCREW PAN HD PHIL M2.5X14	8	
	551125101	WASHER FLAT M2.5	2	
	551125201	WASHER SPLIT LOCK M2.5	9	
	551130101	WASHER FLAT M3	8	
	551130201	WASHER SPLIT LOCK M3	4	
	552425100	NUT HEX M2.5	9	
	552430100	NUT HEX M3	4	
	574409005	WASHER SHOULDER NYLON #4	10	
	575430002	WASHER FLAT .312 OD #4	4	GOES UNDER H7 & H8
	590001014	WIRE TEFLON 19/27 BLK 14	1	

7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	590661014	WIRE TEFLON 19/27 BLU 14	1	
	593910001	CABLE CO-AXIAL RG178B/U	4	
	595003018	SLEEVING SHRINK BLK 3/32"	1	
	707242006	SHIELD, COPPER FOIL FOR HMS603	2	
	707242821	SHIELD (LEFT) 7242ADC	1	SH1
	707242822	SHIELD (RIGHT) 7242ADC	1	SH2
	707242837	HEAT SINK (BOT) 7242ADC	1	H6
	707242838	HEAT SINK (TOP) 7242ADC	1	H2
	707242839	PCB STIFFENER 7242ADC	1	
	717242040	PC BD PREASS'Y 7242ADC	1	
	H7242FLASH	LCC SUBASSEMBLY	8	U4-U7, U17-U20
	HMS603A	HYB SAMPLE/HOLD HMS603A	2	U3, U16
	MTG104	2-PHASE TO 4-PHASE CONV	2	U60, U62
	SM185457101	RES VARI CERMET 100 OHMS	2	R567, R569
	SM185457103	RES VARI CERMET 10 K	12	R259, R284, R620-R627, R629, R631
	SM185457200	RES VARI CERMET 20 OHMS	8	R130, R133, R136, R139, R306, R310, R314, R318
	SM185457201	RES VARI CERMET 200 OHMS	1	R566
	SM200167105	IC 2-3-2 OR/NOR 10H105	2	U26, U41
	SM200167176	IC M-S TYP D FLOP 10H176	16	U27-U34, U43-U50
	SM200178138	IC 3-TO-8-LINE DECODER HCT138	1	U39
	SM207160111	IC CLOCK DRIVER 10E111	6	U40, U42, U69, U70, U55, U56
	SM207178541	IC BUFFER/LINE DR HCT541	4	U35-U38
	SM207244110	IC 8-BIT DAC BT110	4	U51-U54
	SM207961158	IC 5-BIT 2:1 MUX 10E158	5	U57, U58, U61, U71, U72

7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	SM208470324	IC OP AMP LM324M	4	U12-U15
	SM208470358	IC DUAL OP AMP 358D	8	U8-U11, U21-U24
	SM236030099	DIODE SO-PKG BAV99	19	MARKED AS A7X CR1, CR5, CR23-CR28, CR30-CR40
	SM270030092	TRANSISTOR NPN BFR92	2	MARKED AS P1 Q34, Q42
	SM270040092	TRANSISTOR NPN BFR92R	2	MARKED AS P4 Q32, Q44
	SM270132222	TRANSISTOR NPN 2N2222A	10	MARKED AS 1P Q4, Q6, Q11, Q12, Q15, Q16, Q19, Q20, Q23, Q24
	SM275040092	TRANSISTOR PNP BFT92R	1	MARKED AS W4 Q33
	SM275132907	TRANSISTOR PNP 2907A	9	MARKED AS 2F Q3, Q10, Q13, Q14, Q17, Q18, Q21, Q22, Q25
	SM301302001	BEAD FERRITE	5	L21-L24, L26
	SM653181218	RES THICK FILM 1% 15 OHMS	8	R600-R607
	SM653181238	RES THICK FILM 1% 24.3 OHMS	17	R151, R160, R171, R176, R187, R195, R212, R215, R332, R335, R349, R352, R366, R369, R386, R389, R399
	SM653181247	RES THICK FILM 1% 30.1 OHMS	3	R406, R408, R413

7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	SM653181268	RES THICK FILM 1% 49.9 OHMS	46	R88, R93, R142-R145, R148, R152, R168, R172, R189, R190, R194, R198, R202, R206, R214, R218, R309, R313, R317, R321, R323, R324, R327, R329, R333, R343, R346, R350, R368, R372, R388, R392, R438-R441, R444, R460, R575-R579, R588
	SM653181277	RES THICK FILM 1% 61.9 OHMS	24	R153, R154, R173, R174, R191, R192, R203, R204, R251, R254, R263, R266, R289, R292, R299, R302, R325, R326, R342, R344, R358, R359, R376, R377
	SM653181281	RES THICK FILM 1% 68.1 OHMS	34	R52, R65, R74, R79, R96, R105, R114, R127, R164, R165, R180-R183, R207, R208, R339, R340, R356, R357, R361, R362, R381, R382, R451, R475, R492, R499, R494, R493, R498, R497, R496, R495

7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	SM653181297	RES THICK FILM 1% 100 OHMS	168	R50, R51, R53-R64, R66, R67-R73, R75-R78, R80, R81-R85, R94, R95, R97, R98-R104, R106-R113, R115-R126, R128, R129, R131, R132, R134, R135, R137, R138, R140, R141, R307, R308, R311, R312, R315, R316, R319, R320, R445, R447, R456, R457, R461, R462, R468-R472, R481, R491, R500-563, R582, R580, R586, R587, R581, R585, R584, R583, R455, R628, R630
	SM653181305	RES THICK FILM 1% 121 OHMS	11	R26, R37, R38, R40, R454, R458, R459, R574, R593, R594, R596
	SM653181314	RES THICK FILM 1% 150 OHMS	1	R453

7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	SM653181326	RES THICK FILM 1% 200 OHMS	16	R149, R169, R197, R217, R330, R347, R371, R391, R395, R397, R400, R412, R446, R448, R474, R487
	SM653181334	RES THICK FILM 1% 243 OHMS	1	R39
	SM653181336	RES THICK FILM 1% 255 OHMS	1	R36
	SM653181338	RES THICK FILM 1% 267 OHMS	1	R466
	SM653181343	RES THICK FILM 1% 301 OHMS	1	R568
	SM653181347	RES THICK FILM 1% 332 OHMS	4	R608, R609, R612, R613
	SM653181353	RES THICK FILM 1% 383 OHMS	1	R573
	SM653181354	RES THICK FILM 1% 392 OHMS	1	R3
	SM653181362	RES THICK FILM 1% 475 OHMS	17	R14, R398, R401, R410, R414, R463, R464, R467, R595, R570, R565, R25, R41, R610, R235, R611, R271
	SM653181365	RES THICK FILM 1% 511 OHMS	2	R482, R484
	SM653181369	RES THICK FILM 1% 562 OHMS	4	R564, R590, R591, R592
	SM653181377	RES THICK FILM 1% 681 OHMS	1	R396
	SM653181381	RES THICK FILM 1% 750 OHMS	8	R250, R255, R262, R267, R288, R293, R298, R303
	SM653181389	RES THICK FILM 1% 909 OHMS	8	R252, R253, R264, R265, R290, R291, R300, R301
	SM653181393	RES THICK FILM 1% 1.00 K	18	R12, R23, R24, R86, R87, R91, R92, R418, R425, R428, R437, R442, R443, R450, R452, R415, R476, R486

7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	SM653181401	RES THICK FILM 1% 1.21 K	16	R419-R424, R426, R427, R429-R436
	SM653181403	RES THICK FILM 1% 1.27 K	1	R20
	SM653181404	RES THICK FILM 1% 1.30 K	16	R150, R162, R170, R178, R185, R196, R210, R216, R331, R337, R348, R354, R364, R370, R384, R390
	SM653181417	RES THICK FILM 1% 1.78 K	9	R161, R177, R186, R211, R336, R353, R365, R385, R489
	SM653181422	RES THICK FILM 1% 2.00 K	12	R13, R22, R35, R488, R640-R647
	SM653181426	RES THICK FILM 1% 2.21 K	1	R572
	SM653181430	RES THICK FILM 1% 2.43 K	1	R465
	SM653181439	RES THICK FILM 1% 3.01 K	2	R44, R490
	SM653181443	RES THICK FILM 1% 3.32 K	8	R238, R239, R244, R245, R274, R275, R280, R281
	SM653181454	RES THICK FILM 1% 4.32 K	4	R29, R30, R477, R480
	SM653181465	RES THICK FILM 1% 5.62 K	12	R237, R240, R243, R246, R273, R276, R279, R282, R478, R479, R483, R485
	SM653181473	RES THICK FILM 1% 6.81 K	16	R236, R241, R242, R247, R248, R257, R260, R269, R272, R277, R278, R283, R286, R295, R296, R305
	SM653181481	RES THICK FILM 1% 8.25 K	1	R18
	SM653181489	RES THICK FILM 1% 10.0 K	6	R4, R5, R15, R27, R43, R411
	SM653181513	RES THICK FILM 1% 17.8 K	1	R473
	SM653181518	RES THICK FILM 1% 20.0 K	2	R19, R21

7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	SM653181535	RES THICK FILM 1% 30.1 K	1	R16
	SM653181565	RES THICK FILM 1% 61.9 K	1	R17
	SM653181602	RES THICK FILM 1% 150 K	1	R28
	SM653181614	RES THICK FILM 1% 200 K	1	R45
	SM653185039	RES THICK FILM 5% 3.9 OHMS	8	R147, R167, R199, R219, R328, R345, R373, R393
	SM654181000	CHIP JUMPER ZERO OHMS	2	R632, R449
	SM661177104	CAP CERA CHIP .1UF	82	C66, C80-C83, C92-C97, C99-C104, C106-C109, C111-C114, C123-C126, C128-C130, C134, C135, C137, C178-C185, C195, C216, C225-C235, C239, C240, C242-C246, C252, C253, C258-C261, C263, C264, C303, C307, C321, C331-C334, C364, C368, C370, C371
	SM661186100	CAP CERA CHIP 10% 10 PF	1	C133
	SM661186101	CAP CERA CHIP 10% 100 PF	2	C127, C132
	SM661186470	CAP CERA CHIP 10% 47 PF	1	C131
	SM661255471	CAP CERA CHIP 5% 470 PF	1	C33
	SM661276102	CAP CERA CHIP TESTED .001 UF	2	C325, C326

7242ADCA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1105	SM661276103	CAP CERA CHIP TESTED .01 UF	170	C78, C79, C86-C90, C117, C140-C177, C186-C194, C196-C215.C217-C223, C236, C237, C248-C251, C254-C257, C265-C302, C304, C308-C320, C324, C327-C329, C336, C337, C339-C345, C347-C352, C357-C360, C380-C383
	SM661286472	CAP CERA CHIP 10% .0047 UF	2	C322, C323
	SM666247106	CAP MOLD TANT CHIP 10 UF	8	C23-C25, C60, C330, C363, C366, C367

8.2.3 7242AMP PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1026	103317222	CAP CERA MONO 50V 2200 PF	2	C17, C63
	158849011	CAP VARIABLE 2.5 - 10 PF	2	C115, C116
	161225512	RES CARBON FILM 5.1 K	2	R76 R77
	161335104	RES CARBON FILM 100 K	2	
	402110347	CONN BNC STRIPLINE	2	J1,J5
	403119034	HDR DBL ROW RT ANGL 34	2	P1, P2
	408063005	WIREWRAP PIN 1-WRAP	10	
	430542732	RELAY FORM C DPDT 732-2A20	12	U1-U5, U9, U19-U24, U1-U5 U9 U19-U24
	454420032	HDR SOLD TAIL/FEM 32	4	
	500510005	INSULATOR MICA FOR 10-PIN	12	
	550120106	SCREW PAN HD M2X6	8	
	550120510	SCREW FLAT HD PHIL M2X10	9	
	551120101	WASHER FLAT M2	8	
	574209005	WASHER SHOULDER NYLON	8	
	590991022	WIRE TEFLON 7/30 WHT 22	2	
	591101020	WIRE BUS TIN-COPP AWG 20	1	
	595003018	SLEEVING SHRINK BLK 3/32"	1	
	707242932	SHIELD RIGHT 7242	1	
	707242961	SHIELD LEFT 7242	1	
	717242071	PC BD PREASS'Y 7242AMP	1	
	7242SENS	SENSOR ASSEMBLY 7242	2	B1,B2
	C7242AMP2	CABLE ASS'Y FOR 7242AMP	1	
	C7242AMP4	CABLE ASS'Y FOR 7242AMP	1	
	HAT407	HYBRID ATTENUATOR HAT407	2	U10, U25
	HAT408	HYBRID ATTENUATOR HAT408	2	U11, U26
	HAT409	HYBRID ATTENUATOR HAT409	2	U12, U27
	HHZ606	ONE MEG-OHM AMPL ATTENUATOR HHZ606	2	U14, U29
	HII400A-R	HYBRID AMPLIFIER	2	U15, U30

8.2.3 7242AMP PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1026	HIV401A-R	HYBRID AMPLIFIER	2	U16, U31
	PTR403	TRIGGER HYB REPLACEMENT	2	U17, U32
	SM185457103	RES VARI CERMET 10 K	2	R10, R29
	SM185457201	RES VARI CERMET 200 OHMS	2	R52, R54
	SM208470007	IC OP AMP 0P-07	2	U13, U28
	SM208470353	IC DUAL OP AMP LF353	2	U18, U33
	SM240255233	DIODE 6V ZENER MLL5233B	2	CR1, CR2
	SM300337390	INDUCTOR WOUND 39NH	2	L3, L4
	SM301502001	BEAD (FERRITE CHIP)	2	L1, L2
	SM652101122	RES CHIP (E24) 1% 1.2 K	2	R27 R30, R27, R30
	SM653181234	RES THICK FILM 1% 22.1 OHMS	2	R13, R20
	SM653181247	RES THICK FILM 1% 30.1 OHMS	2	R21, R33
	SM653181249	RES THICK FILM 1% 31.6 OHMS	4	R40-R43
	SM653181266	RES THICK FILM 1% 47.5 OHMS	12	R60-R65, R68-R73
	SM653181277	RES THICK FILM 1% 61.9 OHMS	2	R56, R57
	SM653181297	RES THICK FILM 1% 100 OHMS	4	R53, R55, R58, R59
	SM653181314	RES THICK FILM 1% 150 OHMS	4	R14, R19, R34, R37
	SM653181330	RES THICK FILM 1% 221 OHMS	8	R7, R12, R25, R31, R66, R67, R74, R75
	SM653181458	RES THICK FILM 1% 4.75 K	4	R5, R6, R24, R26
	SM653181528	RES THICK FILM 1% 25.5 K	4	R16, R32, R38, R44
	SM653181535	RES THICK FILM 1% 30.1 K	4	R3, R4, R22, R23
	SM653181622	RES THICK FILM 1% 243 K	2	R18, R36
	SM653181657	RES THICK FILM 1% 562 K	2	R17, R39
	SM653181681	RES THICK FILM 1% 1 MEG	6	R8, R9, R11, R28, R100, R200

7242AMP PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1026	SM653265221	RES THICK FILM 5% 220 OHMS	2	R50, R51
	SM661178104	CAP CERA CHIP .1 UF	4	C3, C51, C111, C112
	SM661185681	CAP CERA CHIP 680 PF	4	C41, C84, C40, C83
	SM661186220	CAP CERA CHIP 10% 22 PF	2	C135, C136
	SM661266223	CAP CERA CHIP 10% .022 UF	92	C2, C4, C5, C7-C16, C19, C21, C22, C24, C25, C27-C31, C36-C39, C43-C45, C47, C49, C50, C52, C53, C55-C62, C65, C66, C68, C70-C74, C79-C82, C86-C88, C90, C92-C110, C117-C119, C121-C128, C130-C134
	SM661276102	CAP CERA CHIP TESTED .001 UF	2	C33, C77
	SM661486223	CAP CERA CHIP 10% .022 UF	2	C6, C54
	SM666327225	CAP MOLD TANT CHIP 2.2 UF	10	C18, C23, C26, C32, C46, C64, C67, C69, C75, C89

8.2.4 7242EXTR PARTS LIST

1009	102412180	CAP CERA DISC 100V 18 PF	1	C31
	103296684	CAP CERA MONO 50V .68 UF	1	C20
	208911881	IC VIDEO SYNC SEPARATOR LM1881	1	U6
	402110347	CONN BNC STRIPLINE	1	J1
	403119034	HDR DBL ROW RT ANGL 34	1	J4
	430542732	RELAY FORM C DPDT 732-2A20	1	U1
	454420032	HDR SOLD TAIL/FEM 32	1	
	500510005	INSULATOR MICA FOR 10-PIN	1	
	550120510	SCREW FLAT HD PHIL M2X10	4	
	550120808	SCREW CHEESE HEAD M2X8	3	
	550130106	SCREW PAN HD M3X6	1	
	551120201	WASHER SPLIT LOCK M2	3	
	551130201	WASHER SPLIT LOCK M3	1	
	707242964	BRACKET EXTR 7242	1	
	707242969	BNC MOUNT 7242EXTR	1	
	707242982	SHIELD, EXTR RIGHT 7242	1	
	707242991	SHIELD EXTR LEFT 7242	1	
	717242072	PC BD PREASS'Y 7242EXTR	1	C6
	C7242EXTR	CABLE ASS'Y FOR 7242EXTR	1	
	HHZ606	ONE MEG-OHM AMPL ATTENUATOR HHZ606	1	U2
	PTR403	TRIGGER HYB REPLACEMENT	1	U4
	SM185457103	RES VARI CERMET 10 K	1	R4
	SM200178002	IC 2-INPUT NOR HCT02	1	U7
	SM207171488	IC QUAD LINE DRIVER 1488	2	U9,U10
	SM207770201	IC ANALOG SWITCH DG201	1	U5
	SM207978153	IC 4-INPUT MUX HCT153	1	U8
	SM208470353	IC DUAL OP AMP LF353	1	U3
	SM270330848	TRANSISTOR NPN BC848C	1	Q1
	SM653181234	RES THICK FILM 1% 22.1 OHMS	1	R1
	SM653181266	RES THICK FILM 1% 47.5 OHMS	1	R9
	SM653181297		2	R6,R18
	SM653181338	RES THICK FILM 1% 267 OHMS	1	R7
	SM653181373	RES THICK FILM 1% 619 OHMS	1	R11
	SM653181431	RES THICK FILM 1% 2.49 K	1	R15
	SM653181458	RES THICK FILM 1% 4.75 K	1	R10
	SM653181489	RES THICK FILM 1% 10.0 K	2	R5,R8
	SM653181647	RES THICK FILM 1% 442 K	1	R14
	SM653181652	RES THICK FILM 1% 499 K	1	R2
	SM653181665	RES THICK FILM 1% 681 K	1	R12

	SM653181681	RES THICK FILM 1% 1 MEG	1	R3
	SM653181690	RES THICK FILM 1% 1.24 MEG	1	R13
	SM653265221	RES THICK FILM 5% 220 OHMS	1	R17
	SM661127561	CAP CERA CHIP 20% 560 PF	1	C21
	SM661186150	CAP CERA CHIP 10% 15 PF	1	C6
	SM661266223	CAP CERA CHIP 10% .022 UF	15	C1,C3,C8,C9,C13-C17,C24-C28,C7
	SM661416104	CAP CERA CHIP 10% .1 UF	2	C22,C23
	SM661486223	CAP CERA CHIP 10% .022 UF	1	C2
	SM666327225	CAP MOLD TANT CHIP 2.2 UF	9	C4,C5,C10,C11,C12,C18,C19,C29,C30

8.2.5 7242FPCB PARTS LIST

1002	106438104	CAP CERA MONO .1UF	1
	141264476	CAP TANT DIP 10V 47 UF	2
	141854685	CAP TANT DIP 6.8 UF	1
	161225111	RES CARBON FILM 110 OHMS	24
	161225151	RES CARBON FILM 150 OHMS	20
	184417502	RES VARI COND PLASTIC 5 K	3
	190642151	RESISTOR NETWORK 150 OHMS	1
	256243301	DIODE LED RECTANGULAR RED	2
	256443401	DIODE LED YEL HLMP-0401	29
	412001012	SWITCH ROT NO STOP 12-POS	2
	416161002	SWITCH PUSHBUTTON SPST	16
	454120015	HDR SOLD TAIL/FEM 15	1
	454120030	HDR SOLD TAIL/FEM 30	1
	454120040	HDR SOLD TAIL/FEM 40	1
	454420032	HDR SOLD TAIL/FEM 32	1
	550130106	SCREW PAN HD M3X6	4
	553830108	SPACER HEX M3X8	2
	575470005	WASHER FLAT SIZE #4 NYLON	4
	709400511	COVER FOR L.E.D.	31
	709450523	PUSH SWITCH EXTENDER	16
	717242060	PC BD PREASS'Y 7242FPCB	1
	7242FPCBB	FRONT PNL DUAL POT PC BD ASSY	1
	SM653181314	RES THICK FILM 1% 150 OHMS	6

8.2.6 7242FPCBB PARTS LIST

1002	106438104	CAP CERA MONO .1UF	1	C1
	184447502	RES VARI COND PLASTIC 5 K	1	R1
	454311004	HDR SOLD TAIL/MAIL 4	1	J1
	595901022	SLEEVING TEFLON AWG 22	0	
	717242061	PC BD PREASS'Y 7242FPCBB	1	

8.2.7 7242BFRNT PARTS LIST

1000	530009001	SHIELD (RFI/EMI) FINGER STOCK	1
	536068001	KNOB FOR 6MM SHAFT	2
	536068003	CAP (FOR KNOB 020-2215)	4
	536068004	KNOB FOR 3MM SHAFT	1
	536068005	CAP FOR 020-3215 OR -3415	1
	536168001	KNOB FOR 1/8" SHAFT	3
	550130108	SCREW CYL HD M3X8	7
	551130201	WASHER SPLIT LOCK M3	7
	553530313	SPACER ROUND NYL M3	8
	707242102	FRONT OVERLAY 7242B	1
	707242971	FRONT PANEL 7242	1
	7242FPCB	FRONT PANEL PCB ASS'Y 7242	1

8.2.8 7242ICON PARTS LIST

1005	190001004	RESISTOR NETWORK SPECIAL 10 K	9	U2 U3 U4 U6 U7 U8,U10 U11 U12
	190001005	RESISTOR NETWORK SPECIAL 10 K	3	U1 U5 U9
	208790335	IC TEMPERATURE SENSOR 335	1	CR1
	389440005	POLYETHELENE FOAM TAPE BLACK	0	
	408110009	TERMINAL DOUBLE TURRET	2	TP1,TP2
	429221002	SWITCH THERMAL N.C.	1	S1
	454222048	HDR SOLD TAIL/FEM 48	4	J11-J14
	454321096	HDR SOLD TAIL/FEM 96	12	J21-J24 J31-J34,J41-J44
	717242050	PC BD PREASS'Y 7242ICON	1	

8.2.9 7242SINTFB PARTS LIST

1001	106435102	CAP CERA MONO .001UF	3	C25,C42,C43
	106438104	CAP CERA MONO .1UF	2	C62,C108
	107318104	CAP CERA MONO AXIAL .1UF	90	C2-C6,C8-C10,C12-C17,C26,C29,C31-C39,C44,C45,C48,C50-C57,C63,C66,C68-C107,C110-C116,C19-C23
	141854685	CAP TANT DIP 6.8 UF	4	C1,C60,C61,C109,C18
	142824685	CAP TANT DIP CASE 6.8 UF	4	
	161030000	RES COMP ZERO OHMS	2	R1 R17
	161225102	RES CARBON FILM 1 K	1	R6
	161225303	RES CARBON FILM 30 K	4	R7,R9,R11,R12
	168531489	RES PREC RN55D 10.0 K	5	R2-R5 R16
	190042102	RESISTOR NETWORK 1 K	10	RN1-R10
	200031059	IC HEX BUFF HI-V SN7417N	1	U111
	200031101	IC BIN COUNTER SN74LS393N	1	U42
	200333032	IC QUAD 2-IN OR AS32	2	U1,U81
	200334074	IC D-TYP FLOP AS74	1	U104
	200345138	IC 3-TO-8 DECODER ALS138	4	U25,U26,U80,U96
	200370573	IC D-TYP LATCH 74ALS573	2	U72,U88
	200370574	IC D-TYP FLOP 74ALS574	2	U94,U98
	200380576	IC 8-BIT D-FLOP ALS576	4	U60,U61,U71,U87
	200380823	IC 9-BIT D-FLOP ALS29823	1	U86
	200670273	IC 8-BIT LATCH ALS273	4	U78,U79,U82,U83
	205271050	IC 8192X9-BIT FIFO 7205L50TP	2	U36,U37
	205272832	IC 32K X 8 CMOS RAM HM62832	4	U76,U85,U91,U101
	205298128	IC 128K X 8 SRAM	16	U15-U18,U32-U35,U49-U52,U63-U66
	205372864	IC EE PROM X28C64	1	U106
	205680520	IC PIPELINE REGISTER 29520	2	U19,U20
	205905210	IC CMOS PAL CE22V10Q-25PC	1	U90

1001	205912000	IC GAL16V8A-25LP	1	U22
	205915210	IC CMOS PAL CE22V10Q-25PC	1	U75
	205932000	IC GAL16V8A-25LP	1	U7
	205935210	IC CMOS CE22V10Q-25PC	1	U69
	205942000	IC GAL16V8A-25LP	1	U6
	205955210	IC CMOS PAL CE22V10Q-25PC	1	U57
	205965210	IC CMOS PAL CE22V10Q-25PC	1	U44
	205972211	IC PAL CE22V10H-15PC	2	U112,U114
	205974004	IC CMOS UV PROM 32K X 8 27C2	2	U92,U99
	205975210	IC CMOS PAL CE22V10Q-25PC	1	U41
	205976004	IC CMOS UV PROM 32K X 8 27C2	2	U77,U84
	205992000	IC GAL16V8A-25LP	1	U8
	205994210	IC PAL 22V10	1	U74
	205995210	IC CMOS PAL22V10	1	U58
	205996210	IC CMOS PAL 22V10	1	U67
	207172540	IC BUFF/LINE DRIV ALS540	3	U27,U28,U43
	207172541	IC BUFF/LINE DR ALS541	10	U13,U14,U23,U31,U40,U55,U62,U68,U73,U89
	207181827	IC 10-BIT BUFFER ALS29827	3	U53,U54,U102
	207473645	IC BUS TRANSCEIVER ALS645	16	U2-U5,U9-U12,U21,U38,U39,U47,U48,U56,U103,U110
	207740490	IC DE-BOUNCER 14490	3	U29,U30,U45
	207790161	IC 8-BIT 8-CH DAS 161	2	U59,U70
	208011007	IC DUAL OP AMP LM358N	1	U46
	208130324	IC QUAD OP AMP LM324A	1	U115
	208517705	IC VOLTAGE REG 7705	1	U105
	301016103	INDUCTOR MOLDED 10 UH	1	
	309040040	CRYSTAL OSCILLATOR 40MHZ	1	Y1
	400041024	SOCKET IC SOLD TAIL DIP-24	6	
	400360028	SOCKET IC SOLD TAIL DIP-28	4	
	400413068	IC SOCKET GRID TYPE 68-PIN	4	U93 U100 U107 U113,U93,U100,U107,U113
	408072001	TERMINAL SINGLE TURRET	3	TP1-TP3
	433221004	FUSE PICO II 125V 1 AMP	2	F2,F3
	433225001	FUSE PICO II 125V 5 AMP	1	F1
	454510030	HDR SOLD TAIL/MALE 30	1	P4
	454510080	HDR SOLD TAIL/MALE 80	1	P3
	454610048	HDR SOLD TAIL/MALE 48	1	P11
	454612096	HDR SOLD TAIL/MALE 96	4	P1,P21,P31,P41

	454710004	HDR SOLD TAIL/MALE 4	1	
	550125110	SCREW PAN HD M2.5X10	2	
	707242951	CONN BRACKET 7242	1	
	717242001	7242SINTF	1	
	MNX401	IC MIN-MAX GATE ARRAY MNX401	2	U107,U113
	SM227060320	IC DIGITAL SIG PROC 320C25	2	U93,U100

8.2.10 7242BMEM PARTS LIST

1003	106348224	CAP CERA MONO .22UF	1	C199
	106433271	CAP CERA MONO 270PF	1	C221
	106433561	CAP CERA MONO 560PF	2	C200,C201
	106435102	CAP CERA MONO .001UF	1	C202
	106445222	CAP CERA MONO 2200PF	1	C188
	141264476	CAP TANT DIP 10V 47 UF	1	C70
	141854685	CAP TANT DIP 6.8 UF	1	C233
	146674157	CAP MINI ALUM 20% 150 UF	13	C203,C205,C206,C208,C210,C212,C213,C214,C223,C224,C227,C228,C,229
	161335100	RES CARBON FILM 10 OHMS	2	R172,R173
	161335101	RES CARBON FILM 100 OHMS	2	R195,R250
	161335102	RES CARBON FILM 1 K	1	R179
	161335201	RES CARBON FILM 200 OHMS	1	R189
	161335271	RES CARBON FILM 270 OHMS	1	R191
	161335470	RES CARBON FILM 47 OHMS	3	R200,R174,R175
	161335680	RES CARBON FILM 68 OHMS	1	R202
	161445010	RES CARBON FILM 1 OHM	2	R181,R182
	161445100	RES CARBON FILM 10 OHMS	1	R171
	161445101	RES CARBON FILM 100 OHMS	1	R170
	161445150	RES CARBON FILM 15 OHMS	2	R178,R201
	161445331	RES CARBON FILM 330 OHMS	1	R190
	161445510	RES CARBON FILM 51 OHMS	2	R168,R169
	161555510	RES COMP 1W 5% 51 OHMS	1	R176
	168531362	RES PREC RN55D 475 OHMS	1	R180
	180247102	RES VARI CERMET 1 K	1	R158
	180247202	RES VARI CERMET 2 K	1	R166
	208164002	IC VOLT REG POS MC78L15CG	1	U169
	208590431	IC ADJ SHUNT REG TL431	3	U170,U173,U174
	208713844	IC PWM CONTROLLER 3844	1	U176

1003	208743825	IC PWM CONTROLLER 3825	1	U175
	230110005	DIODE SWITCHING 1N4448	2	CR3,CR4
	235982545	DIODE RECTIFIER MBR2545CT	1	U172,U172
	240513248	DIODE ZENER 18V 5% 1N5248B	2	CR10,CR14
	253040545	DIODE SCHOTTKY MBR1545CT	1	U171
	253050817	DIODE HOT CARRIER 1N5817	3	CR2,CR11,CR12
	260022017	OPTICAL ISOLATOR CNY17-II	2	U140,U166
	280170104	TRANSISTOR FET N VN0104N3	1	Q7
	280190530	TRANSISTOR FET "N" IRF530	3	Q4-Q6
	302071111	INDUCTOR (SW REG) 110 UH	1	L1
	302382120	INDUCTOR WOUND 12 UH	2	L2,L3
	385020180	INSULATING FILM KAPTON	0	
	400410084	IC SOCKET GRID TYP 84-POS	8	
	408063005	WIREWRAP PIN 1-WRAP	1	TP1
	433220001	FUSE PICO II 125V 10 AMP	2	F1,F2
	433220002	FUSE PICO II 125V 3 AMP	1	F3
	433225001	FUSE PICO II 125V 5 AMP	2	F4,F5
	440202401	TRANSFORMER 7242MEM-T1	1	T2
	440202402	TRANSFORMER 7242MEM-T2	1	T3
	440242403	TRANSFORMER 7242MEM-T3	1	L4
	440282001	TRANSFORMER 72XXCT-T1	1	T1
	454610048	HDR SOLD TAIL/MALE 48	1	P12
	454611032	CONN MALE MIXED 32	1	P113
	454612096	HDR SOLD TAIL/MALE 96	3	P22,P32,P42
	454910002	CONTACT (HI-CURRENT) INSERT	3	J1-J3
	485024017	BUMPER ROUND BLK PLASTIC	1	
	500120002	TRANSIPAD "LARGE"	1	U169
	500460006	INSULATOR THERMALFILM	2	
	500860302	INSULATOR FOR TO-220	3	
	505051001	HEAT SINK FOR SCR LO PROF	2	H4
	505051015	HEATSINK FOR TO-220 0.375" HIGH	3	
	505070002	HEAT SINK FOR TO-220	2	
	550125110	SCREW PAN HD M2.5X10	2	
	550130110	SCREW CYL HD M3X10	2	
	550130112	SCREW PAN HD M3X12	3	
	551130101	WASHER FLAT M3	5	
	551130201	WASHER SPLIT LOCK M3	5	
	552430100	NUT HEX M3	5	
	574409005	WASHER SHOULDER NYLON #4	5	
	590001018	WIRE TEFLON 19/30 BLK 18	2	

1003	591692330	WIRE BLU/WHT TW PR SOLID AWG 30	10	
	593910001	CABLE CO-AXIAL RG178B/U	1	
	707242070	HEATSINK FOR 7242BMEMA	1	
	707242951	CONN BRACKET 7242	1	
	717234020	PC BD PREASS'Y 7234MEM	1	
	C7242MEMA	CABLE ASS'Y FOR 7242MEM	1	
	C7242MEMB	CABLE ASS'Y FOR 7242MEM	1	
	C7242MEMC	CABLE ASS'Y FOR 7242MEM	1	
	MDX802	1-TO-8 MONO DEMUX	8	U3,U17,U31,U45,U70,U85,U99,U113
	SM200172000	IC 2-INPUT NAND 74F00	1	U69
	SM200172074	IC D-TYP FLOP 74F74	8	U8,U22,U36,U50,U75,U90,U104,U118
	SM200470373	IC TRANSPARENT LATCH FCT373	16	U15,U16,U29,U30,U43,U44,U57,U58,U83,U84,U97,U98,U111,U112,U125,U126
	SM205238408	IC 8K X 8-BIT RAM	64	U4-U7,U11-U14,U18-U21,U25-U28,U32-U35,U39-U42,U46-U49,U53-U56,U71-U74,U79-U82,U86-U89,U93-U96,U100-U103,U107-U110,U114-U117,U121-U124
	SM205921016	IC PAL 16L8D	2	U64,U66
	SM207160111	IC CLOCK DRIVER 10E111	3	U62,U63,U65

1003	SM207180244	IC BUFFER/LINE DR FCT244	20	U9,U10,U23,U24,U37,U38,U51,U52,U59,U60,U67,U68,U77,U78,U91,U92,U105,U106,U119,U120
	SM207367125	IC TRANSLATOR 10H125	1	U61
	SM207460116	IC LINE RECEIVER 10H116	1	U127
	SM236030099	DIODE SO-PKG BAV99	3	MARKED AS A7 CR1,CR5,CR9
	SM270132222	TRANSISTOR NPN 2N2222A	2	MARKED AS 1P Q3,Q8
	SM275132907	TRANSISTOR PNP 2907A	2	MARKED AS 2F Q1,Q2
	SM653181201	RES THICK FILM 1% 10 OHMS	2	R260,R261
	SM653181277	RES THICK FILM 1% 61.9 OHMS	2	R36,R37
	SM653181285	RES THICK FILM 1% 75 OHMS	98	R23,R24,R33,R35,R38,R63-R83,R85-R152,R167,R1008,R1009
	SM653181326	RES THICK FILM 1% 200 OHMS	2	R262,R263
	SM653181354	RES THICK FILM 1% 392 OHMS	1	R187
	SM653181362	RES THICK FILM 1% 475 OHMS	1	R198
	SM653181393	RES THICK FILM 1% 1.00 K	5	R1,R199,R219,R257,R220
	SM653181403	RES THICK FILM 1% 1.27 K	1	R212
	SM653181418	RES THICK FILM 1% 1.82 K	1	R177
	SM653181422	RES THICK FILM 1% 2.00 K	3	R185,R186,R188
	SM653181439	RES THICK FILM 1% 3.01 K	1	R255
	SM653181443	RES THICK FILM 1% 3.32 K	1	R258
	SM653181450	RES THICK FILM 1% 3.92 K	2	R192,R193
	SM653181454	RES THICK FILM 1% 4.32 K	1	R196
	SM653181458	RES THICK FILM 1% 4.75 K	1	R197
	SM653181481	RES THICK FILM 1% 8.25 K	1	R231
	SM653181489	RES THICK FILM 1% 10.0 K	10	R210,R211,R214,R221,R230,R252,R256,R259,R1001,R213

1003	SM653181518	RES THICK FILM 1% 20.0 K	2	R183,R184,
	SM653181528	RES THICK FILM 1% 25.5 K	1	R233
	SM653181535	RES THICK FILM 1% 30.1 K	1	R217
	SM653181554	RES THICK FILM 1% 47.5 K	1	R232
	SM653181565	RES THICK FILM 1% 61.9 K	1	R215
	SM653181602	RES THICK FILM 1% 150 K	2	R194,R253
	SM653181614	RES THICK FILM 1% 200 K	1	R254
	SM661186100	CAP CERA CHIP 10% 10 PF	1	C57
	SM661186101	CAP CERA CHIP 10% 100 PF	2	C240,C245
	SM661186470	CAP CERA CHIP 10% 47 PF	1	C231
	SM661186471	CAP CERA CHIP 10% 470 PF	1	C56
	SM661276102	CAP CERA CHIP TESTED .001 UF	4	C1,C189,C234, C250
	SM661276103	CAP CERA CHIP TESTED .01 UF	173	C3-C16,C21-C33,C38,C39,C42,C44-C55,C60-C69,C76-C91,C93-C187,C246-C249,C251-C255
	SM661286473	CAP CERA CHIP 10% .047 UF	1	C232
	SM661407104	CAP CERA CHIP TESTED .1 UF	9	C190-C196,C198,C222
	SM666217106	CAP MOLD TANT CHIP 10 UF	4	C43,C73,C74,C75
	SM666247106	CAP MOLD TANT CHIP 10 UF	6	C215-C220

8.2.11 7242BMEMA PARTS LIST

ECO	PART #	DESCRIPTION	QTY	REMARKS
1003	106348224	CAP CERA MONO .22UF	1	C199
	106433271	CAP CERA MONO 270PF	1	C221
	106433561	CAP CERA MONO 560PF	2	C200,C201
	106435102	CAP CERA MONO .001UF	1	C202
	106445222	CAP CERA MONO 2200PF	1	C188
	141264476	CAP TANT DIP 10V 47 UF	1	C70
	141854685	CAP TANT DIP 6.8 UF	1	C233
	146674157	CAP MINI ALUM 20% 150 UF	13	C203,C205,C206,C208,C210,C212,C213,C214,C223,C224,C227,C228,C,229
	161335100	RES CARBON FILM 10 OHMS	2	R172,R173
	161335101	RES CARBON FILM 100 OHMS	2	R195,R250
	161335102	RES CARBON FILM 1 K	1	R179
	161335201	RES CARBON FILM 200 OHMS	1	R189
	161335271	RES CARBON FILM 270 OHMS	1	R191
	161335470	RES CARBON FILM 47 OHMS	3	R200,R174,R175
	161335680	RES CARBON FILM 68 OHMS	1	R202
	161445010	RES CARBON FILM 1 OHM	2	R181,R182
	161445100	RES CARBON FILM 10 OHMS	1	R171
	161445101	RES CARBON FILM 100 OHMS	1	R170
	161445150	RES CARBON FILM 15 OHMS	2	R178,R201
	161445331	RES CARBON FILM 330 OHMS	1	R190
	161445510	RES CARBON FILM 51 OHMS	2	R168,R169
	161555510	RES COMP 1W 5% 51 OHMS	1	R176
	168531362	RES PREC RN55D 475 OHMS	1	R180
	180247102	RES VARI CERMET 1 K	1	R158
	180247202	RES VARI CERMET 2 K	1	R166
	208164002	IC VOLT REG POS MC78L15CG	1	U169
	208590431	IC ADJ SHUNT REG TL431	3	U170,U173,U174
	208713844	IC PWM CONTROLLER 3844	1	U176
	208743825	IC PWM CONTROLLER 3825	1	U175
	230110005	DIODE SWITCHING 1N4448	2	CR3,CR4
	235982545	DIODE RECTIFIER MBR2545CT	1	U172,U172
	240513248	DIODE ZENER 18V 5% 1N5248B	2	CR10,CR14
	253040545	DIODE SCHOTTKY MBR1545CT	1	U171

	253050817	DIODE HOT CARRIER 1N5817	3	CR2,CR11,CR 12
	260022017	OPTICAL ISOLATOR CNY17-II	2	U140,U166
	280170104	TRANSISTOR FET N VN0104N3	1	Q7
	280190530	TRANSISTOR FET "N" IRF530	3	Q4-Q6
	302071111	INDUCTOR (SW REG) 110 UH	1	L1
	302382120	INDUCTOR WOUND 12 UH	2	L2,L3
	385020180	INSULATING FILM KAPTON	0	
	400410084	IC SOCKET GRID TYP 84-POS	8	
	408063005	WIREWRAP PIN 1-WRAP	1	TP1
	433220001	FUSE PICO II 125V 10 AMP	2	F1,F2
	433220002	FUSE PICO II 125V 3 AMP	1	F3
	433225001	FUSE PICO II 125V 5 AMP	2	F4,F5
	440202401	TRANSFORMER 7242MEM-T1	1	T2
	440202402	TRANSFORMER 7242MEM-T2	1	T3
	440242403	TRANSFORMER 7242MEM-T3	1	L4
	440282001	TRANSFORMER 72XXCT-T1	1	T1
	454610048	HDR SOLD TAIL/MALE 48	1	P12
	454611032	CONN MALE MIXED 32	1	P113
	454612096	HDR SOLD TAIL/MALE 96	3	P22,P32,P42
	454910002	CONTACT (HI-CURRENT) INSERT	3	J1-J3
	485024017	BUMPER ROUND BLK PLASTIC	1	
	500120002	TRANSIPAD "LARGE"	1	U169
	500460006	INSULATOR THERMALFILM	2	
	500860302	INSULATOR FOR TO-220	3	
	505051001	HEAT SINK FOR SCR LO PROF	2	H4
	505051015	HEATSINK FOR TO-220 0.375" HIGH	3	
	505070002	HEAT SINK FOR TO-220	2	
	550125110	SCREW PAN HD M2.5X10	2	
	550130110	SCREW CYL HD M3X10	2	
	550130112	SCREW PAN HD M3X12	3	
	551130101	WASHER FLAT M3	5	
	551130201	WASHER SPLIT LOCK M3	5	
	552430100	NUT HEX M3	5	
	574409005	WASHER SHOULDER NYLON #4	5	
	590001018	WIRE TEFLON 19/30 BLK 18	2	
	591692330	WIRE BLU/WHT TW PR SOLID AWG 30	10	
	593910001	CABLE CO-AXIAL RG178B/U	1	
	707242070	HEATSINK FOR 7242BMEMA	1	
	707242951	CONN BRACKET 7242	1	
	717234020	PC BD PREASS'Y 7234MEM	1	

	C7242MEMA	CABLE ASS'Y FOR 7242MEM	1	
	C7242MEMB	CABLE ASS'Y FOR 7242MEM	1	
	C7242MEMC	CABLE ASS'Y FOR 7242MEM	1	
	MDX802	1-TO-8 MONO DEMUX	8	U3,U17,U31,U45,U70,U85,U99,U113
	SM200172000	IC 2-INPUT NAND 74F00	1	U69
	SM200172074	IC D-TYP FLOP 74F74	8	U8,U22,U36,U50,U75,U90,U104,U118
	SM200470373	IC TRANSPARENT LATCH FCT373	16	U15,U16,U29,U30,U43,U44,U57,U58,U83,U84,U97,U98,U111,U112,U125,U126
	SM205238258	IC 32K X 8 SRAM 58258AJ-20	64	U4-U7,U11-U14,U18-U21,U25-U28,U32-U35,U39-U42,U46-U49,U53-U56,U71-U74,U79-U82,U86-U89,U93-U96,U100-U103,U107-U110,U114-U117,U121-U124
	SM205921016	IC PAL 16L8D	2	U64,U66
	SM207160111	IC CLOCK DRIVER 10E111	3	U62,U63,U65
	SM207180244	IC BUFFER/LINE DR FCT244	20	U9,U10,U23,U24,U37,U38,U51,U52,U59,U60,U67,U68,U77,U78,U91,U92,U105,U106,U119,U120
	SM207367125	IC TRANSLATOR 10H125	1	U61
	SM207460116	IC LINE RECEIVER 10H116	1	U127
	SM236030099	DIODE SO-PKG BAV99	3	MARKED AS

				A7 CR1,CR5,CR9
	SM270132222	TRANSISTOR NPN 2N2222A	2	MARKED AS 1P Q3,Q8
	SM275132907	TRANSISTOR PNP 2907A	2	MARKED AS 2F Q1,Q2
	SM653181201	RES THICK FILM 1% 10 OHMS	3	R260,R261,R1 000
	SM653181277	RES THICK FILM 1% 61.9 OHMS	2	R36,R37
	SM653181285	RES THICK FILM 1% 75 OHMS	98	R23,R24,R33, R35,R38,R63- R83,R85- R152,R1008,R 1009
	SM653181326	RES THICK FILM 1% 200 OHMS	2	R262,R263
	SM653181354	RES THICK FILM 1% 392 OHMS	1	R187
	SM653181362	RES THICK FILM 1% 475 OHMS	1	R198
	SM653181393	RES THICK FILM 1% 1.00 K	5	R1,R199,R219, R257,R220
	SM653181403	RES THICK FILM 1% 1.27 K	1	R212
	SM653181418	RES THICK FILM 1% 1.82 K	1	R177
	SM653181422	RES THICK FILM 1% 2.00 K	3	R185,R186,R1 88
	SM653181439	RES THICK FILM 1% 3.01 K	1	R255
	SM653181443	RES THICK FILM 1% 3.32 K	1	R258
	SM653181450	RES THICK FILM 1% 3.92 K	2	R192,R193
	SM653181454	RES THICK FILM 1% 4.32 K	1	R196
	SM653181458	RES THICK FILM 1% 4.75 K	1	R197
	SM653181481	RES THICK FILM 1% 8.25 K	1	R231
	SM653181489	RES THICK FILM 1% 10.0 K	9	R210,R211,R2 14,R221,R230, R252,R259,R2 13,R256
	SM653181518	RES THICK FILM 1% 20.0 K	2	R184,R183
	SM653181528	RES THICK FILM 1% 25.5 K	1	R233
	SM653181535	RES THICK FILM 1% 30.1 K	1	R217
	SM653181554	RES THICK FILM 1% 47.5 K	1	R232
	SM653181565	RES THICK FILM 1% 61.9 K	1	R215
	SM653181602	RES THICK FILM 1% 150 K	2	R194,R253
	SM653181614	RES THICK FILM 1% 200 K	1	R254
	SM661186100	CAP CERA CHIP 10% 10 PF	1	C57
	SM661186101	CAP CERA CHIP 10% 100 PF	2	C240,C245
	SM661186470	CAP CERA CHIP 10% 47 PF	1	C231

	SM661186471	CAP CERA CHIP 10% 470 PF	1	C56
	SM661276102	CAP CERA CHIP TESTED .001 UF	4	C1,C189,C234, C250
	SM661276103	CAP CERA CHIP TESTED .01 UF	173	C3-C16,C21-C33,C38,C39, C42,C44-C55,C60-C69,C76-C91,C93-C187,C246-C249,C251-C255
	SM661286473	CAP CERA CHIP 10% .047 UF	1	C232
	SM661407104	CAP CERA CHIP TESTED .1 UF	9	C190-C196,C198,C222
	SM666217106	CAP MOLD TANT CHIP 10 UF	4	C43,C73,C74, C75
	SM666247106	CAP MOLD TANT CHIP 10 UF	6	C215-C220

8.2.12 7234TMB PARTS LIST

1105	106433271	CAP CERA MONO 270PF	3	C2,C3,C8
	106433471	CAP CERA MONO 470PF	2	C13,C14
	106438104	CAP CERA MONO .1UF	1	C18
	106445222	CAP CERA MONO 2200PF	1	C1
	141854685	CAP TANT DIP 6.8 UF	1	C5
	146674157	CAP MINI ALUM 20% 150 UF	10	C15-C17,C19,C23-C26,C32,C33
	161225391	RES CARBON FILM 390 OHMS	1	
	161225510	RES CARBON FILM 51 OHMS	1	
	161335100	RES CARBON FILM 10 OHMS	2	R9,R10
	161335201	RES CARBON FILM 200 OHMS	1	R8
	161335271	RES CARBON FILM 270 OHMS	1	R7
	161335391	RES CARBON FILM 390 OHMS	1	R22
	161335470	RES CARBON FILM 47 OHMS	2	R24,R27
	161445101	RES CARBON FILM 100 OHMS	2	R26,R29
	161445150	RES CARBON FILM 15 OHMS	1	R30
	161445221	RES CARBON FILM 220 OHMS	2	R5,R6
	168009901	RES PREC .1% 900 OHMS	1	R91
	168009902	RES PREC .1% 9.0 K	1	R92
	168139297	RES RN55E .1% 100 OHMS	1	R100
	180247501	RES VARI CERMET 500 OHMS	1	R33
	207115002	IC MONO BUFF/AMPL 5002	2	U9,U30
	207280703	IC 16-BIT DAC703	1	U74
	208122337	IC ADJ -VOLT REG LM337T	2	U7,U12
	208164002	IC VOLT REG POS MC78L15CG	1	U1
	208570317	IC ADJ +V REG LM317	2	U8,U10
	208590431	IC ADJ SHUNT REG TL431	1	U4
	208743825	IC PWM CONTROLLER 3825	1	U2
	240513248	DIODE ZENER 18V 5% 1N5248B	3	CR7,CR14,CR15
	253050817	DIODE HOT CARRIER 1N5817	2	CR11,CR12
	253072110	DIODE SCHOTTKY 21DQ10	4	CR1,CR2,CR4,CR5
	253083110	DIODE SCHOTTKY 31DQ10	4	CR3,CR6,CR9,CR10
	260022017	OPTICAL ISOLATOR CNY17-II	1	U3
	280190530	TRANSISTOR FET "N" IRF530	2	Q3,Q4
	290199020	DELAY LINE 2.0 NS	3	D2,D5,D6
	290199025	DELAY LINE 2.5 NS	2	D3,D4
	290199029	DELAY LINE 2.9 NS	2	D8,D9

	290199030	DELAY LINE 3.0 NS	1	
	290199049	DELAY LINE 4.9 NS	1	D11
	300050001	CHOKE FERRITE SINGLE LEAD	3	L1,L2,L4
	300050002	CHOKE FERRITE SINGLE LEAD	2	L204 L211
	300480001	COIL BOBBIN (SINGLE SECT)	2	D7,D10
	301016222	INDUCTOR MOLDED 2.20 UH	2	L200 L207
	301016822	INDUCTOR MOLDED 8.2 UH	2	L9,L10
	301486224	INDUCTOR SHIELDED 220 UH	7	L6,L7,L8,L11,L 12,L13,L14
	302382120	INDUCTOR WOUND 12 UH	1	L3
	309040100	CRYSTAL OSCILLATOR 100MHZ	1	U84
	402610003	CONN CO-AX PC MTG SMB	8	J3-J10
	403110020	HEADER ASSEMBLY 20-PIN	1	P4
	403119034	HDR DBL ROW RT ANGL 34	3	P1-P3
	433220001	FUSE PICO II 125V 10 AMP	1	F3
	433220002	FUSE PICO II 125V 3 AMP	2	F6,F8
	433220004	FUSE PICO II 125V 1.5 AMP	2	F4,F5
	433222005	FUSE PICO II 125V 2 AMP	2	F1,F7
	433225001	FUSE PICO II 125V 5 AMP	1	F2
	440202501	TRANSFORMER 7242TMB-T1	1	T1
	440242502	TRANSFORMER 7242TMB-T2	1	T2
	440282001	TRANSFORMER 72XXCT-T1	1	T3
	454610048	HDR SOLD TAIL/MALE 48	1	P13
	454612096	HDR SOLD TAIL/MALE 96	3	P23,P33,P43
	500120002	TRANSIPAD "LARGE"	1	U1
	500460006	INSULATOR THERMALFILM	4	Q3 Q4 U10 U12
	505051002	HEAT SINK (DBL) FOR TO-220	1	HS1
	505070002	HEAT SINK FOR TO-220	2	Q3 Q4
	519230001	SNAP RIVET NYLON	2	U7,U8
	550130110	SCREW CYL HD M3X10	4	Q3 Q4 U10 U12
	551130101	WASHER FLAT M3	4	Q3 Q4 U10 U12
	551130201	WASHER SPLIT LOCK M3	4	Q3 Q4 U10 U12
	552430100	NUT HEX M3	4	Q3 Q4 U10 U12
	574409005	WASHER SHOULDER NYLON #4	4	Q3 Q4 U10 U12
	591692330	WIRE BLU/WHT TW PR SOLID AWG 30	16	D1,D7,D10
	593910001	CABLE CO-AXIAL RG178B/U	5	J1,J2,J11,J12,J

				13,J14
	717234070	PC BD PREASS'Y 7234TMB	1	
	HTD405	TIME DIGITIZER	1	U75
	MCL404	IC MEM GATE ARRAY MCL404	1	U72
	SM185248104	RES VARI CERMET 100 K	2	R108,R139
	SM200160101	IC OR-NOR GATE 10H101	1	U107
	SM200160402	IC 16-BIT SCALER MCT402	7	U16,U17,U32, U45,U59,U65, U66
	SM200167105	IC 2-3-2 OR/NOR 10H105	7	U111,U116,U1 33,U134,U136, U144,U152
	SM200167107	IC 2-IN EXCL OR/NOR 10H107	2	U115,U143
	SM200167117	IC OR-AND/OR-AND-INV 10H117	3	U110,U128,U1 29
	SM200167121	IC OR-AND/OR-AND-INV 10H121	4	U103,U108,U1 09,U131
	SM200167131	IC M-S TYP D FLOP 10H131	17	U104,U114,U1 18,U120,U122-U126,U130,U1 35,U139,U140, U146,U147,U1 51,U155
	SM200167210	IC OR GATE 10H210	1	U141
	SM200170032	IC 2-IN OR GATE 74F32	2	U22,U55
	SM200172011	IC 3-INPUT AND 74F11	1	U56
	SM200172074	IC D-TYP FLOP 74F74	1	U47
	SM200172374	IC D-TYP FLOP 74F374	2	U58,U62
	SM200176074	IC D-TYP FLOP 74HC74	4	U27,U31,U33, U76
	SM200176564	IC D-TYP FLOP HC564	3	U67,U157,U15 8
	SM200178000	IC 2-INPUT NAND HCT00	2	U40.U46
	SM200178004	IC HEX INVERTER HCT04	2	U37,U77
	SM200178008	IC 2-INPUT AND HCT08	1	U41
	SM200178138	IC 3-TO-8-LINE DECODER HCT138	2	U63,U68
	SM200178574	IC D-TYP FLOP HCT574	13	U14,U18,U23, U34,U42,U48, U57,U70,U71, U73,U89,U90, U95
	SM200267016	IC BINARY COUNTER 10H016	7	U113,U119,U1 32,U138,U142,

				U145,U150
	SM200276161	IC 4-BIT COUNTER HC161	2	U78,U79
	SM200278040	IC COUNTER HCT4040	4	U85-U88
	SM205930210	IC PAL 22V10 CMOS	1	U38
	SM205932210	IC PAL 22V10 CMOS	1	U51
	SM205933210	IC PAL 22V10 CMOS	1	U52
	SM205938210	IC PAL 22V10	1	U39
	SM207171488	IC QUAD LINE DRIVER 1488	3	U19,U29,U43
	SM207178541	IC BUFFER/LINE DR HCT541	7	U81-U83,U91-U94
	SM207182240	IC BUFFER/LINE DRIVER F240	1	U54
	SM207188241	IC BUFF/DRIVR/RCVR HCT241	4	U13,U21,U26,U36
	SM207367124	IC TRANSLATOR 10H124	1	U154
	SM207367125	IC TRANSLATOR 10H125	5	U105,U106,U112,U148,U153
	SM207460116	IC LINE RECEIVER 10H116	8	U100-U102,U117,U121,U127,U137,U149
	SM207770201	IC ANALOG SWITCH DG201	4	U20,U50,U61,U69
	SM207978157	IC 2-INPUT MUX HCT157	1	U96
	SM208470027	IC SINGLE OP AMP OP-27	2	U11,U35
	SM208470353	IC DUAL OP AMP LF353	7	U15,U25,U44,U53,U60,U64,U80
	SM208470358	IC DUAL OP AMP 358D	1	U156
	SM208870339	IC VOLT COMPARATOR 339	1	U28
	SM232120056	DIODE ARRAY BAW56	2	CR17,CR18
	SM236030099	DIODE SO-PKG BAV99	4	CR8,CR13,CR20,CR21
	SM270030093	TRANSISTOR NPN BFR93	3	Q5-Q7
	SM270132222	TRANSISTOR NPN 2N2222A	1	Q1
	SM275030092	TRANSISTOR PNP BFT92	2	Q8,Q9
	SM275132907	TRANSISTOR PNP 2907A	1	Q2
	SM289772003	TRANSISTOR ARRAY 2003	2	U24,U49
	SM301302001	BEAD FERRITE	4	L39,L220,L221,L222
	SM301502001	BEAD (FERRITE CHIP)	18	L5,L201,L202,L203,L205,L206,L208,L209,L210,L212,L213,L2

				14,L215-L219,L223
	SM651181103	RES CHIP THIN FILM .1% 10 K	4	R371,R372,373,R375
	SM653181201	RES THICK FILM 1% 10 OHMS	2	R304,R307
	SM653181218	RES THICK FILM 1% 15 OHMS	4	R40,R41,R61,R76
	SM653181261	RES THICK FILM 1% 42.2 OHMS	2	R324,R337
	SM653181268	RES THICK FILM 1% 49.9 OHMS	38	R204,R205,R208,R209,R212,R213,R255,R259,R262,R263,R265,R269,R271,R273,R276,R279,R280,R296,R299,R302,R306,R308,R310,R311,R320,R322,R327,R330,R331,R332,R334,R347,R348,R355,R356,R357,R358,R386
	SM653181277	RES THICK FILM 1% 61.9 OHMS	6	R257,R258,R277,R278,R314,R316
	SM653181285	RES THICK FILM 1% 75 OHMS	1	R336
	SM653181293	RES THICK FILM 1% 90.9 OHMS	1	R319
	SM653181297	RES THICK FILM 1% 100 OHMS	91	R202,R203,R206,R207,R210,R211,R214,R217,R219,R226-R235,R238,R239-R249,R252,R254,R256,R260,R261,R264,R266-R268,R270,R272,R274,R275,R281-R283,R285-R287,R290,R2

				93,R294,R295, R297,R298,R3 00,R301,R305, R309,R312,R3 13,R315,R323, R325,R326,R3 28,R329,R333, R338-R345,R349,R3 50-R354,R359,R3 61,R362,R363, R370,R374,R3 87,R253
	SM653181303	RES THICK FILM 1% 115 OHMS	2	R35,R36
	SM653181305	RES THICK FILM 1% 121 OHMS	2	R44,R409
	SM653181326	RES THICK FILM 1% 200 OHMS	2	R52,R78
	SM653181334	RES THICK FILM 1% 243 OHMS	1	R376
	SM653181338	RES THICK FILM 1% 267 OHMS	2	R317,R318
	SM653181343	RES THICK FILM 1% 301 OHMS	4	R103,R104,R2 88,R289
	SM653181358	RES THICK FILM 1% 432 OHMS	2	R34,R38
	SM653181362	RES THICK FILM 1% 475 OHMS	4	R4,R21,R37.R 43
	SM653181369	RES THICK FILM 1% 562 OHMS	2	R42,R45
	SM653181370	RES THICK FILM 1% 576 OHMS	1	R321
	SM653181393	RES THICK FILM 1% 1.00 K	69	R15,R18,R20, R66,R71,R80, R101,R102,R1 06,R109,R110, R113,R116,R1 18,R120,R121, R123,R125,R1 27,R130,R131, R134,R136,R1 37,R141,R143, R146,R147,R1 54,R155,R156, R157-R159,R200,R2 01,R215,R218, R221-R225,R236,R2 50,R251,R291,

				R335,R346,R360,R364,R365-R369,R378-R385,R388,R410-R413
	SM653181403	RES THICK FILM 1% 1.27 K	1	R13
	SM653181422	RES THICK FILM 1% 2.00 K	8	R3,R16,R56,R58,R68,R69,R105,R107
	SM653181426	RES THICK FILM 1% 2.21 K	2	R23,R416
	SM653181431	RES THICK FILM 1% 2.49 K	2	R67,R72
	SM653181439	RES THICK FILM 1% 3.01 K	3	R39,R53,R77
	SM653181451	RES THICK FILM 1% 4.02 K	53	R48,R49,R54,R55,R62,R79,R81,R111,R112,R114,R115,R117,R119,R122,R124,R126,R128,R129,R132,R133,R135,R138,R140,R142,R144,R145,R148-R153,R216,R220,R237,R292,R389,R390-R395,R397,R398,R399-R404,R414,R415
	SM653181458	RES THICK FILM 1% 4.75 K	1	R32
	SM653181489	RES THICK FILM 1% 10.0 K	25	R1,R2,R12,R25,R28,R95,R96,R97,R98,R377,R396,R99,R63,R65,R82,R83,R90,R93,R94,R405,R406,R407,R408,R86,R89
	SM653181513	RES THICK FILM 1% 17.8 K	1	R14
	SM653181518	RES THICK FILM 1% 20.0 K	4	R11,R17,R64,R70
	SM653181535	RES THICK FILM 1% 30.1 K	3	R19,R57,R59

	SM653181626	RES THICK FILM 1% 267 K	1	R284
	SM653181631	RES THICK FILM 1% 301 K	1	R31
	SM653181727	RES THICK FILM 1% 3.01 MEG	1	R303
	SM661186101	CAP CERA CHIP 10% 100 PF	4	C6,C252,C255, C272
	SM661186181	CAP CERA CHIP 10% 180 PF	1	C495
	SM661186220	CAP CERA CHIP 10% 22 PF	3	C345,C403,C4 04
	SM661186272	CAP CERA CHIP 10% 2700 PF	2	C35,C447
	SM661186330	CAP CERA CHIP 10% 33 PF	2	C155,C164
	SM661186560	CAP CERA CHIP 10% 56 PF	1	C399
	SM661186680	CAP CERA CHIP 10% 68 PF	1	C494
	SM661276102	CAP CERA CHIP TESTED .001 UF	42	C34,C80,C162, C170,C185,C2 28,C229,C243, C,246- C248,C253,C2 57,C,258,C269, C274- C277,C286,C3 07,C315,C319, C324,C332,C3 33,C334,C339, C343,C344,C3 53,C354,C364, C371,C374,C3 75,C379,C382, C389,C398,C4 05,C406
	SM661276103	CAP CERA CHIP TESTED .01 UF	309	C36,C37,C41, C44,C53- C65,C69- C78,C81,C82- C86,C88,C89, C91,C92- C97,C100,C10 1,C102- C113,C115,C1 16,C118- C130,C132,C1 34- C141,C144,C1 46,C147- C154,C163,C1

				65,C167-C169,C171-C184,C225-C227,C230-C242,C244,C245,C249-C251,C254,C256,C259-C268,C270,C271,C273,C278,C279-C285,C287-C289,C292-C306,C308-C314,C316-C318,C320-C323,C325-C331,C335-C338,C340-C342,C346-C352,C355-C363,C365-C370,C372,C373,C376-C378,C380,C381,C383-C388,C390-C397,C401,C402,C407-C412,C414-C436,C438-C444,C448,C450,C451-C453,C456-C472,C474-C480
	SM661407104	CAP CERA CHIP TESTED .1 UF	17	C4,C7,C10,C11,C31,C38,C47,C49,C52,C67,C79,C483,C485,C486,C487,C489,C490
	SM661726103	CAP CERA CHIP 10% .01 UF	12	C50,C51,C66,C68,C87,C90,

				C98,C99,C114, C117,C131,C1 33
	SM666247106	CAP MOLD TANT CHIP 10 UF	42	C437,C449,C4 73,C481,C9,C1 2,C20,C21,C22 ,C27- C30,C39,C40, C42,C43,C45, C46,C48,C142, C143,C145,C1 56,C157- C161,C166,C4 00,C413,C445, C446,C454,C4 55,C482,C484, C488,C493,C4 91,C492

8.2.13 7242TAMP PARTS LIST

1004	106438104	CAP CERA MONO .1UF	4	C1,C2,C5,C6
	142824685	CAP TANT DIP CASE 6.8 UF	4	C3,C4,C7,C8
	161020470	RES CARBON COMP 47 OHMS	34	R1-R17,R19-R35
	161225101	RES CARBON FILM 100 OHMS	2	R18,R36
	300030001	BEAD SHIELDING FERRITE	2	L1 L3
	301016222	INDUCTOR MOLDED 2.20 UH	2	L2 L4
	454320034	HDR SOLD TAIL/FEM 34	2	J3,J4
	454320038	HDR SOLD TAL/FEM 38	2	J1,J2
	454990000	KEYING PLUG	8	
	707242777	INSULATOR 1/32" G-10	1	
	717242080	PC BD PREASS'Y 7242TAMP	1	